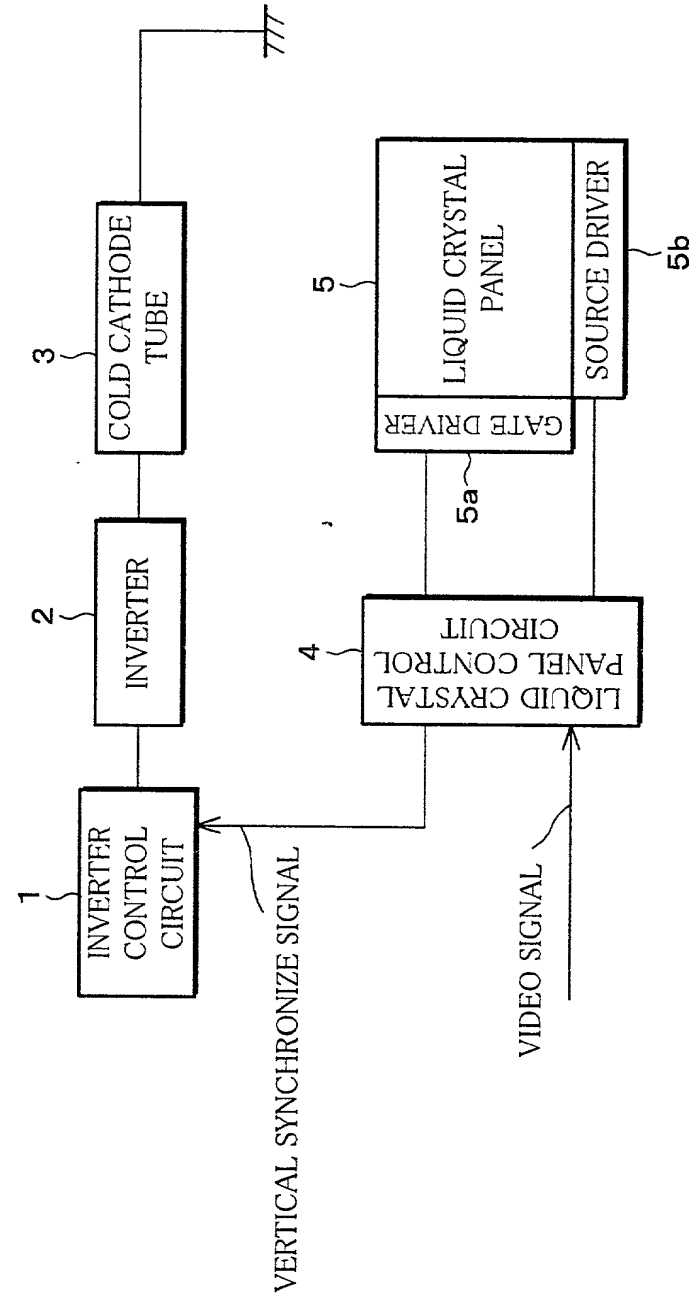
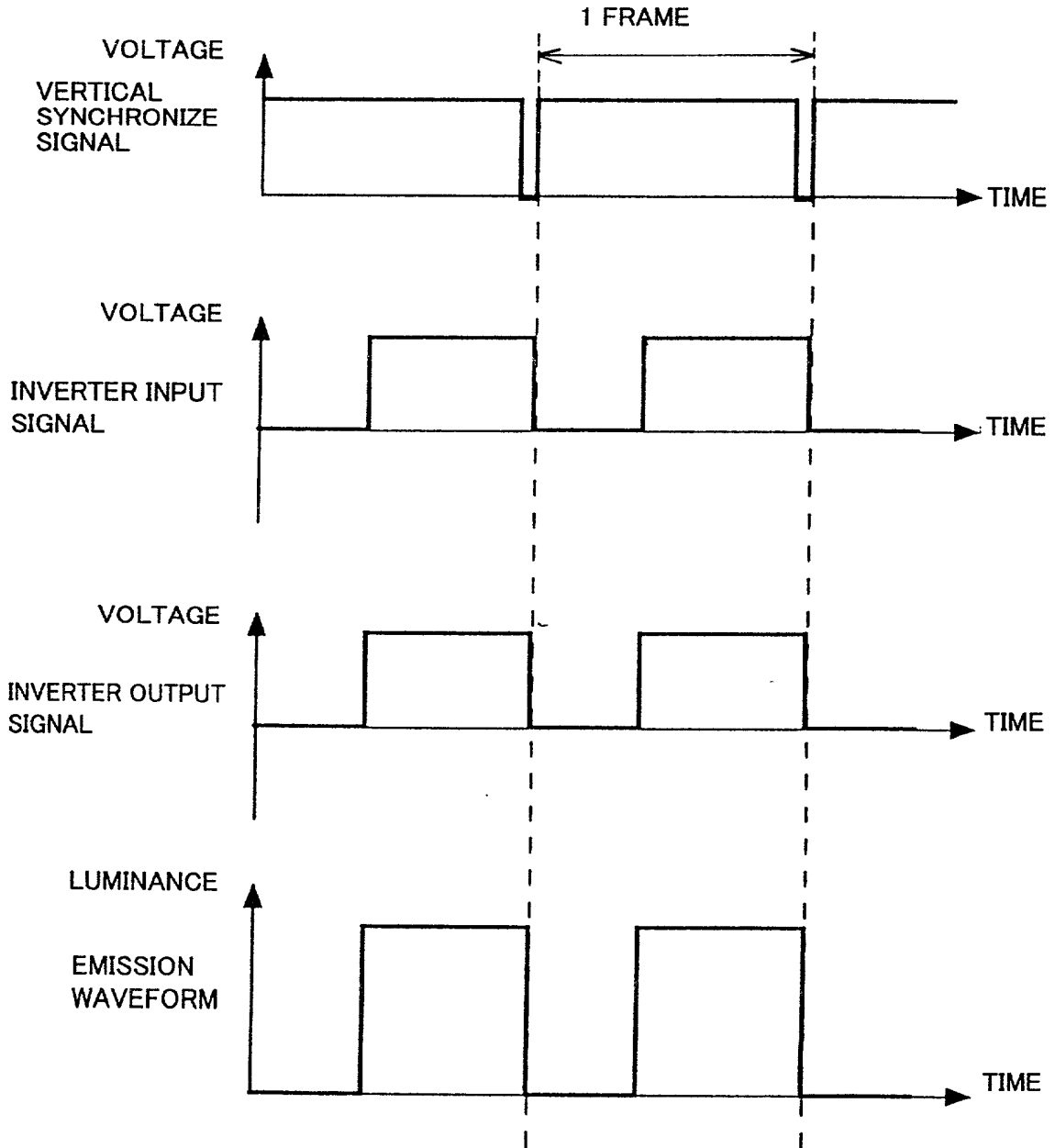


FIG. 1



F I G . 2



F I G . 3

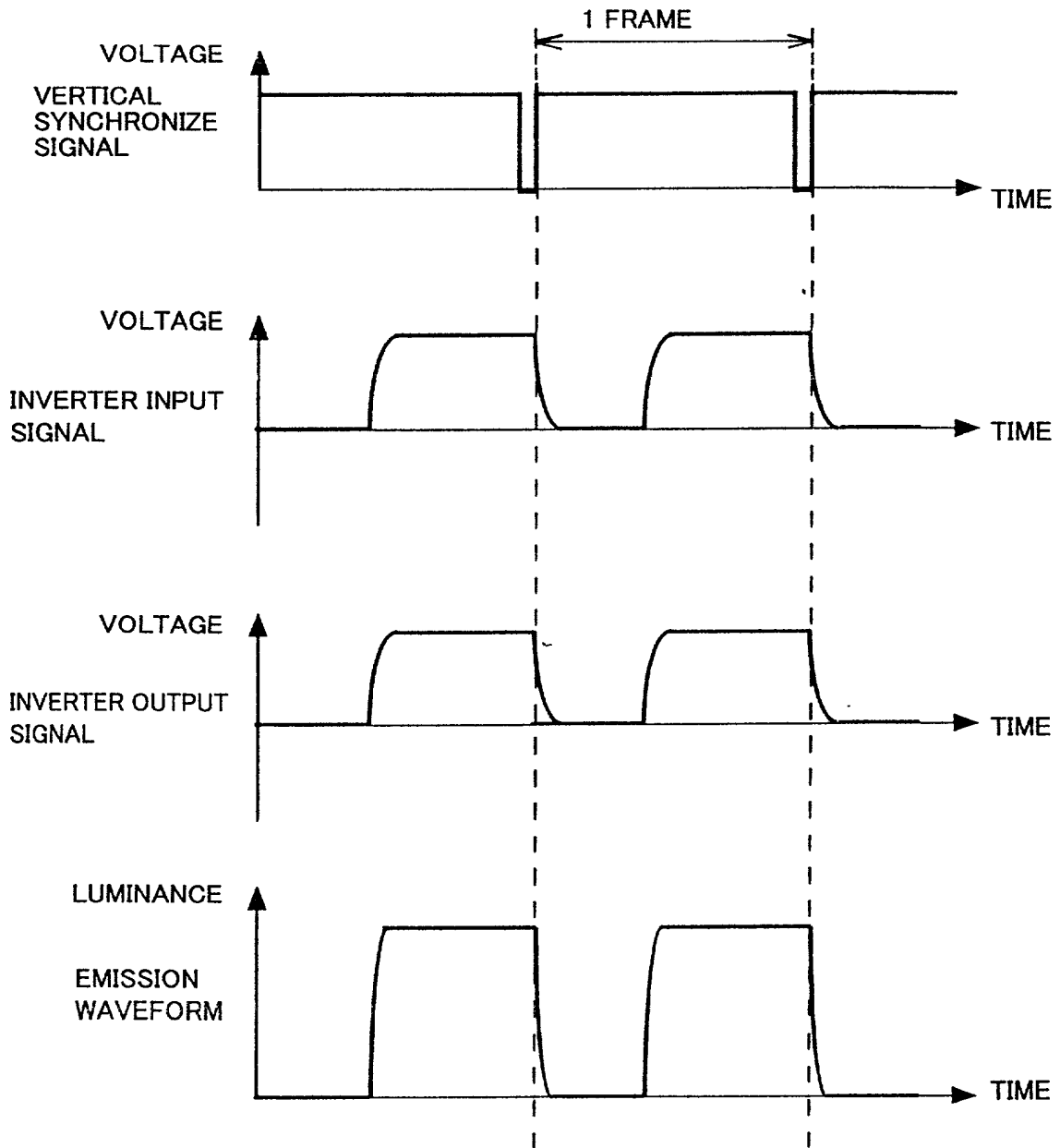


FIG. 4

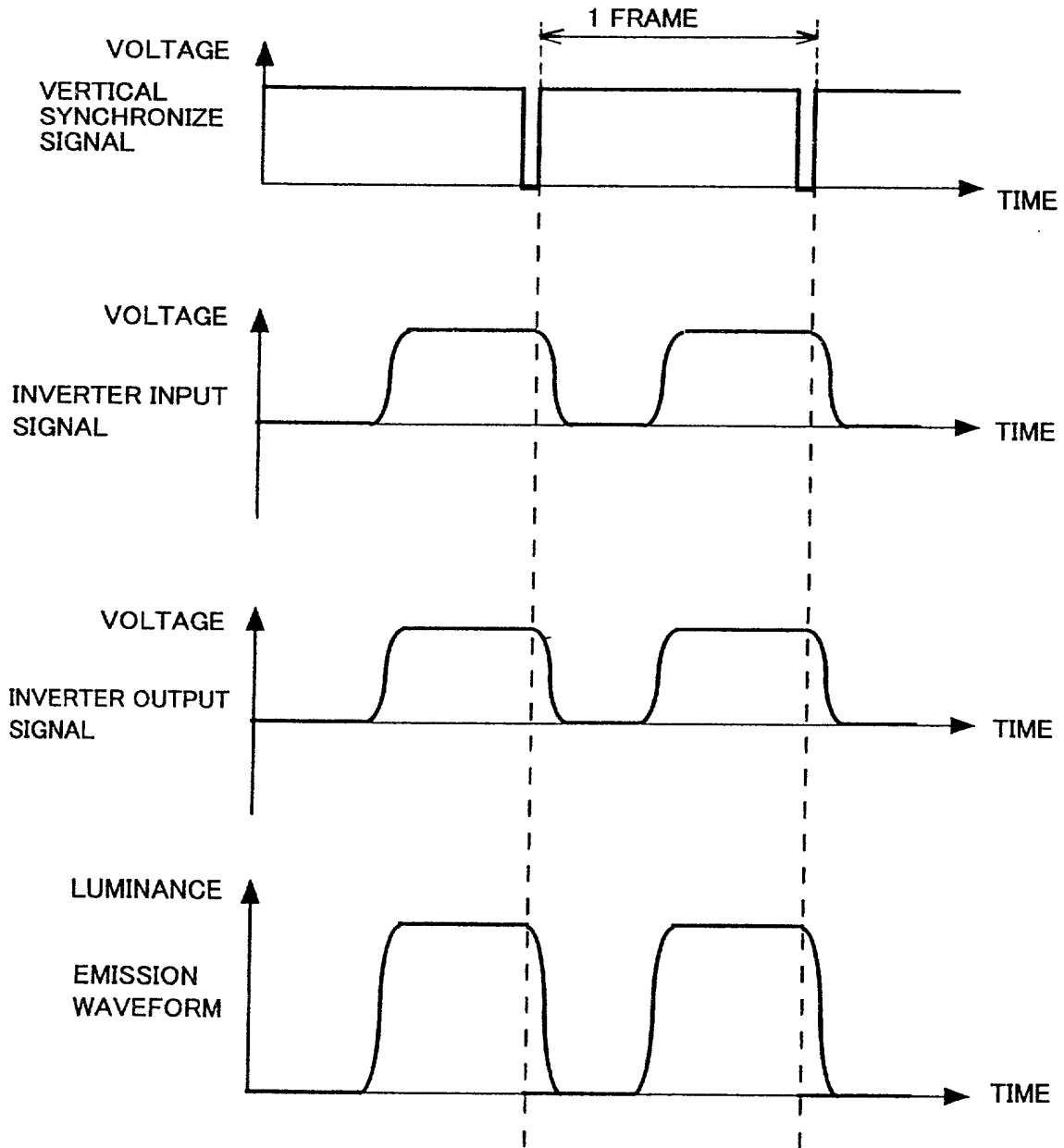


FIG. 5

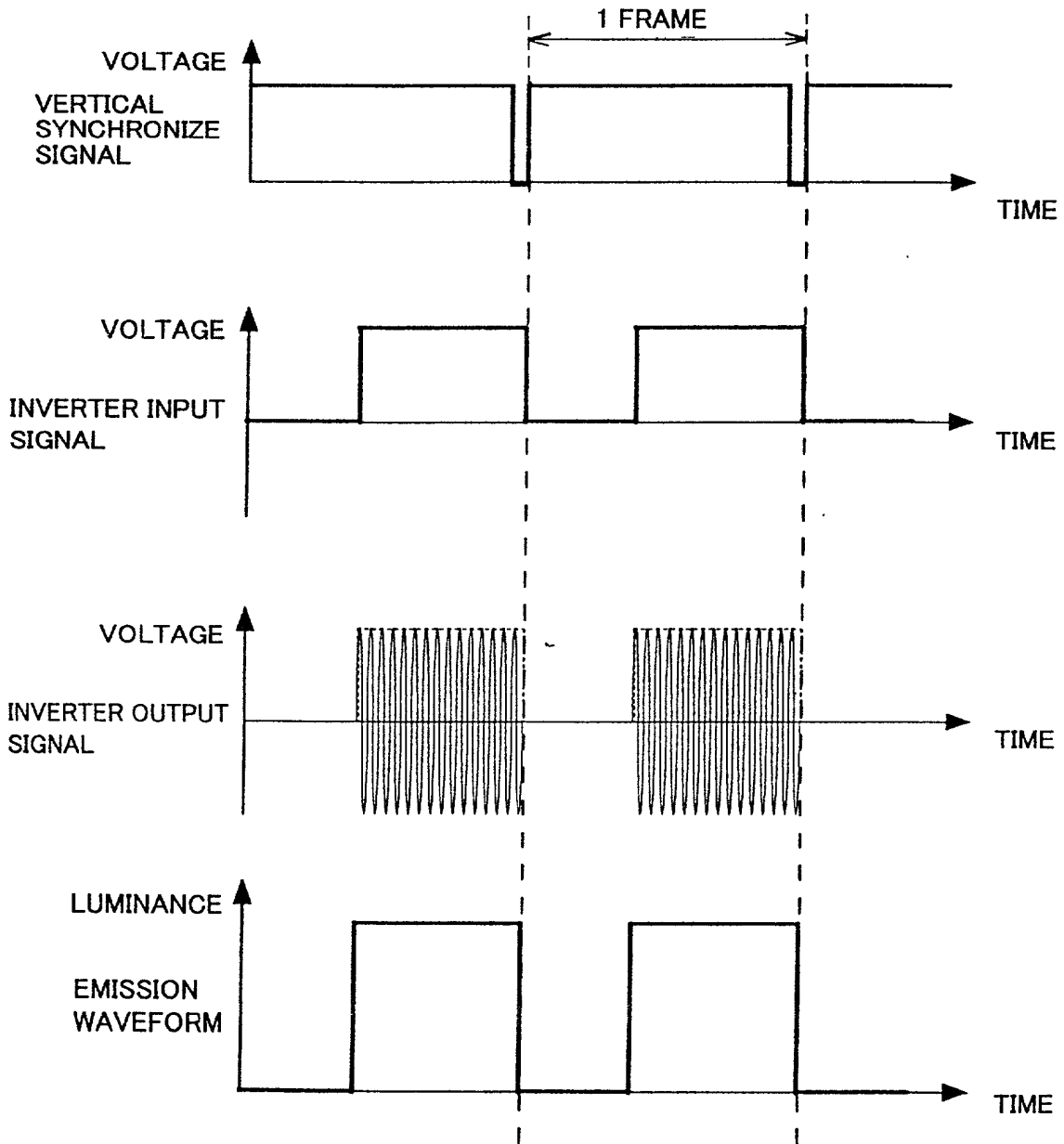
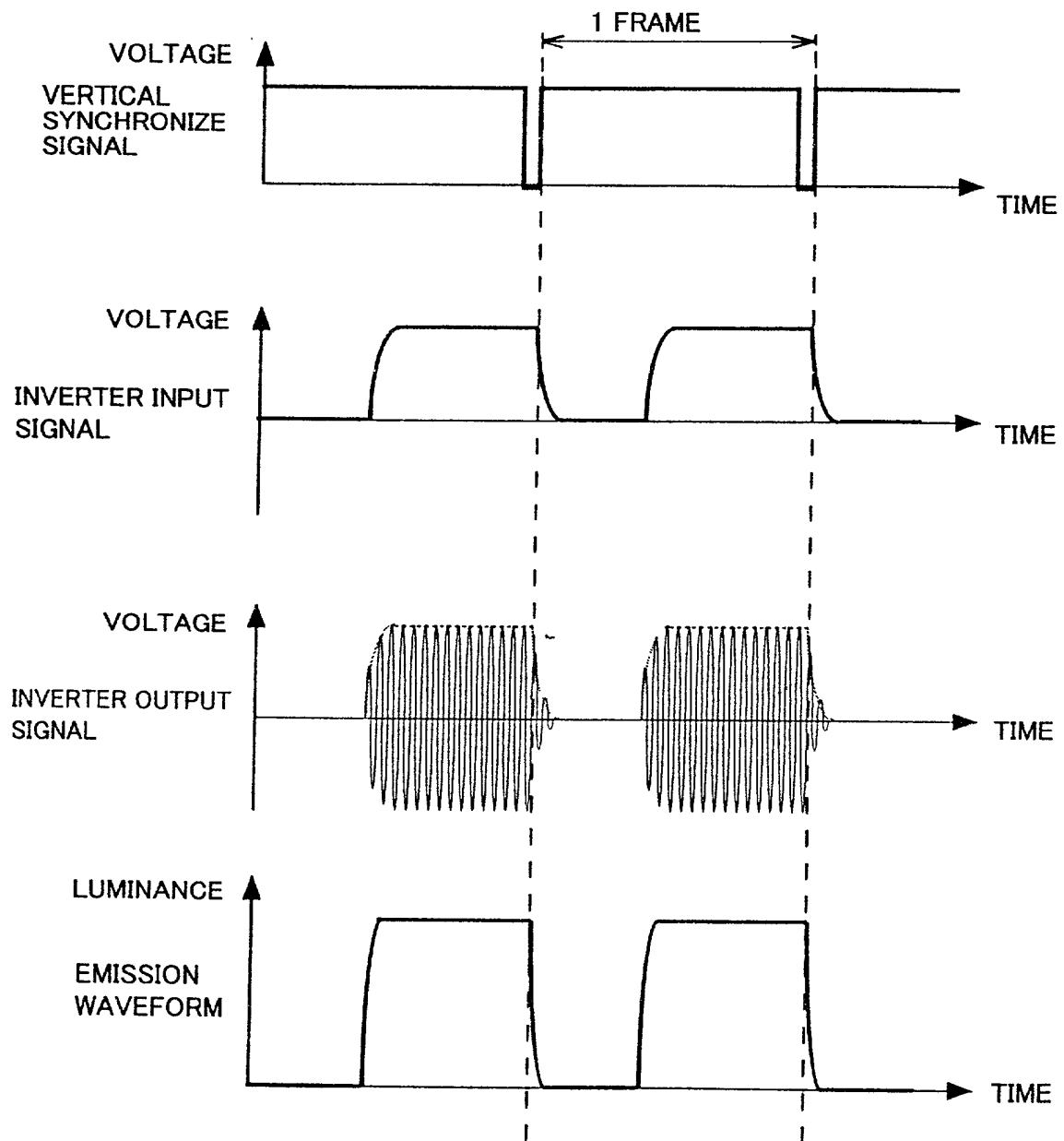


FIG. 6



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FIG. 7

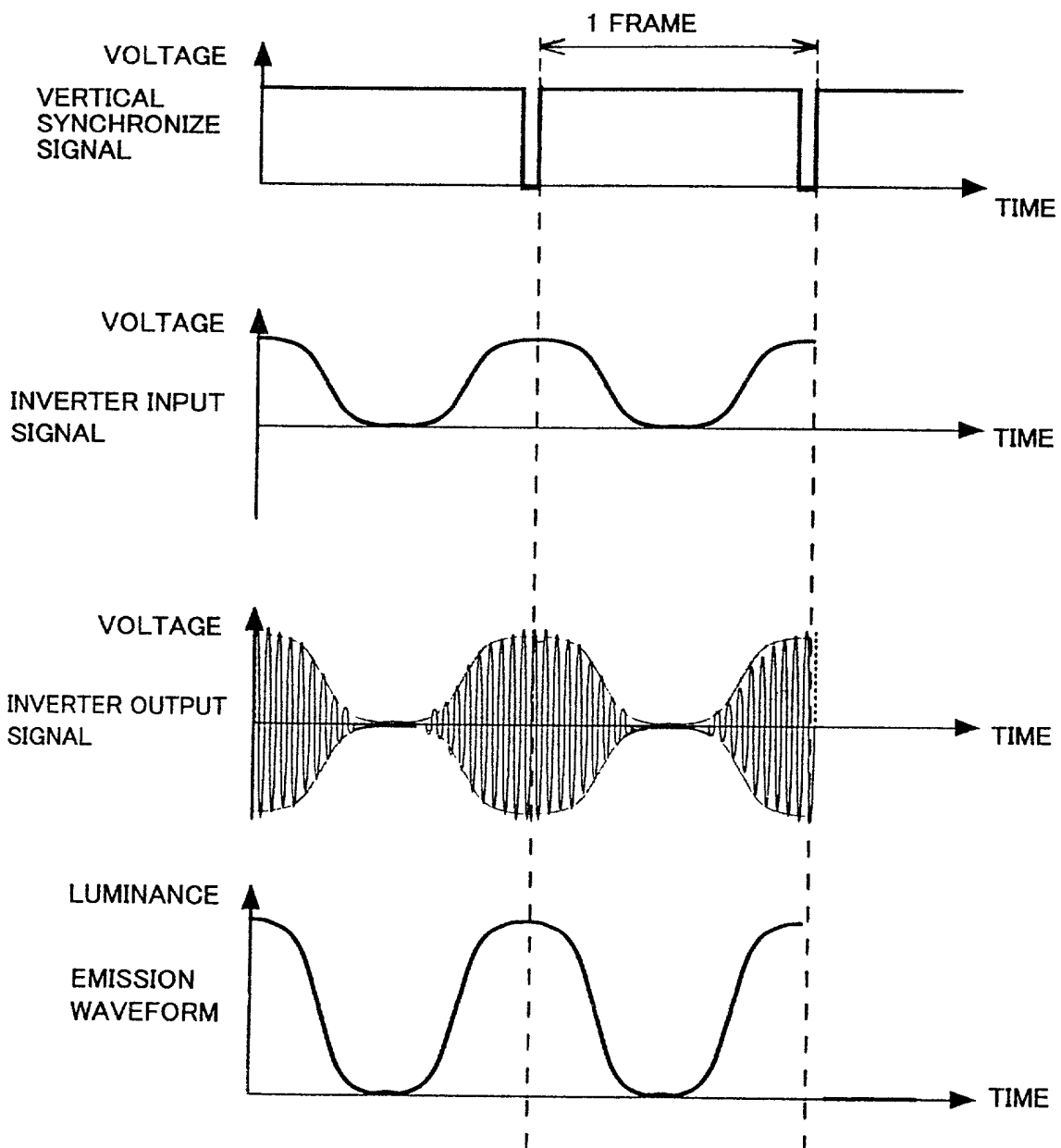


FIG. 8

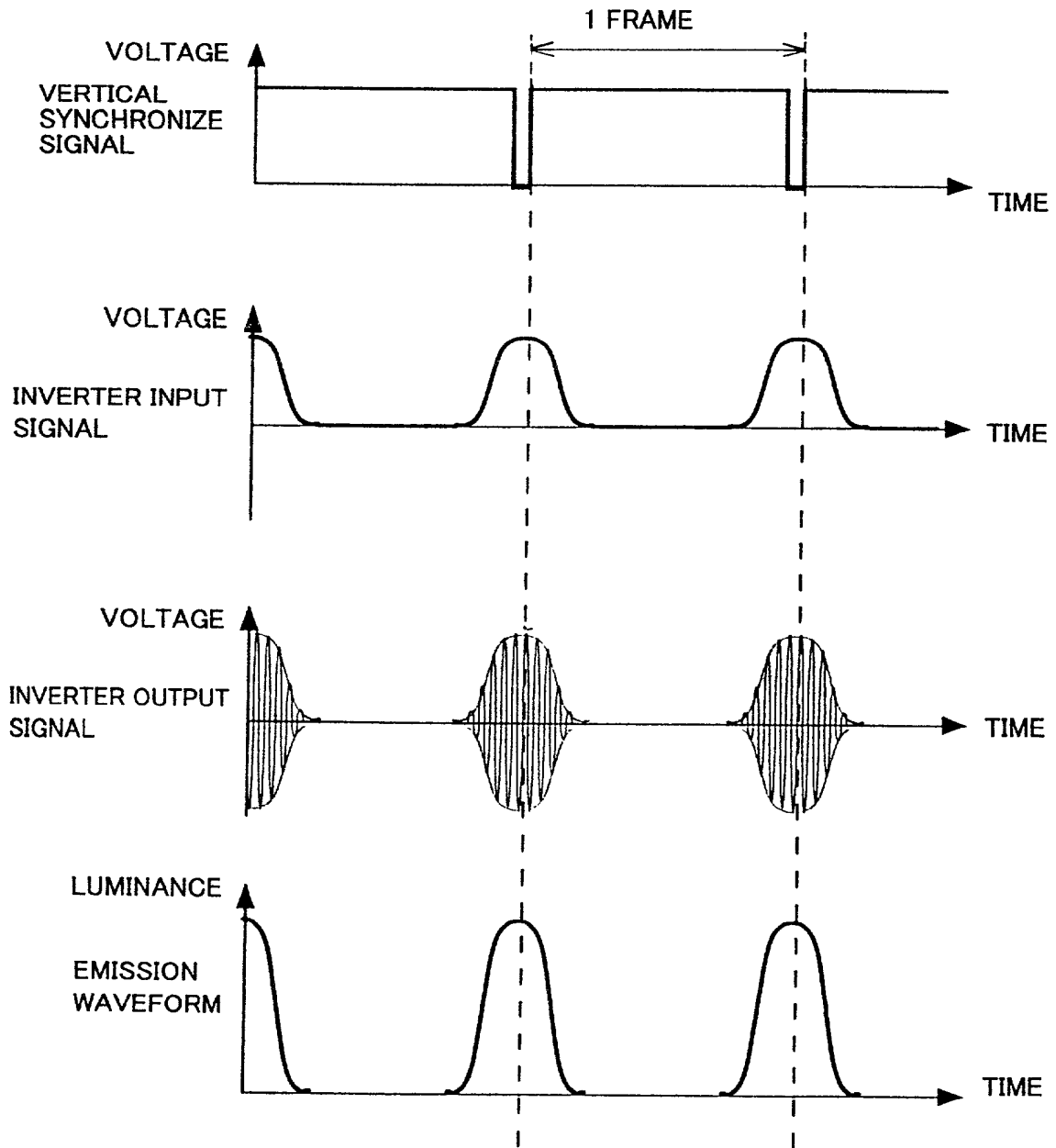


FIG. 9

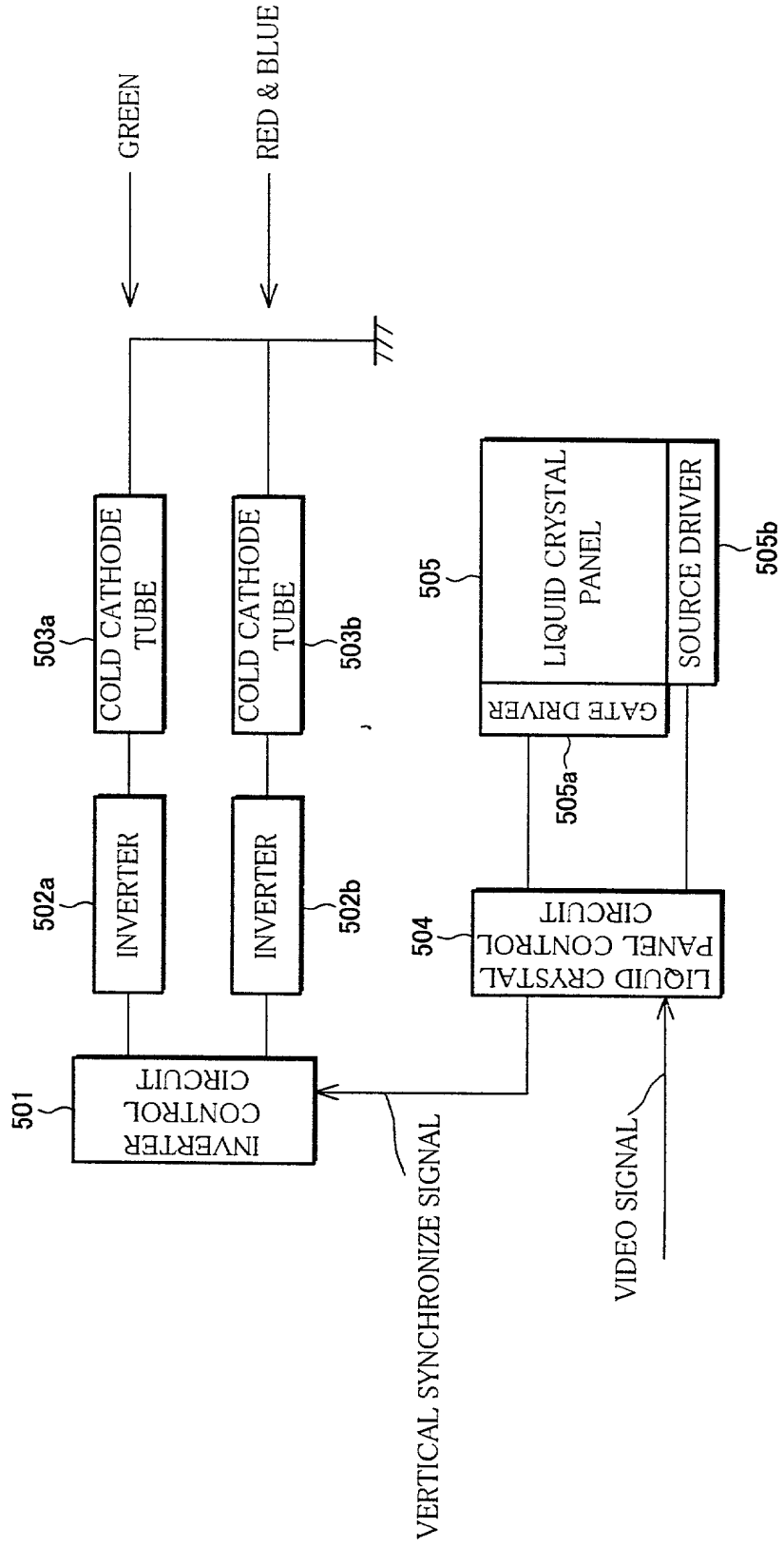


FIG. 10

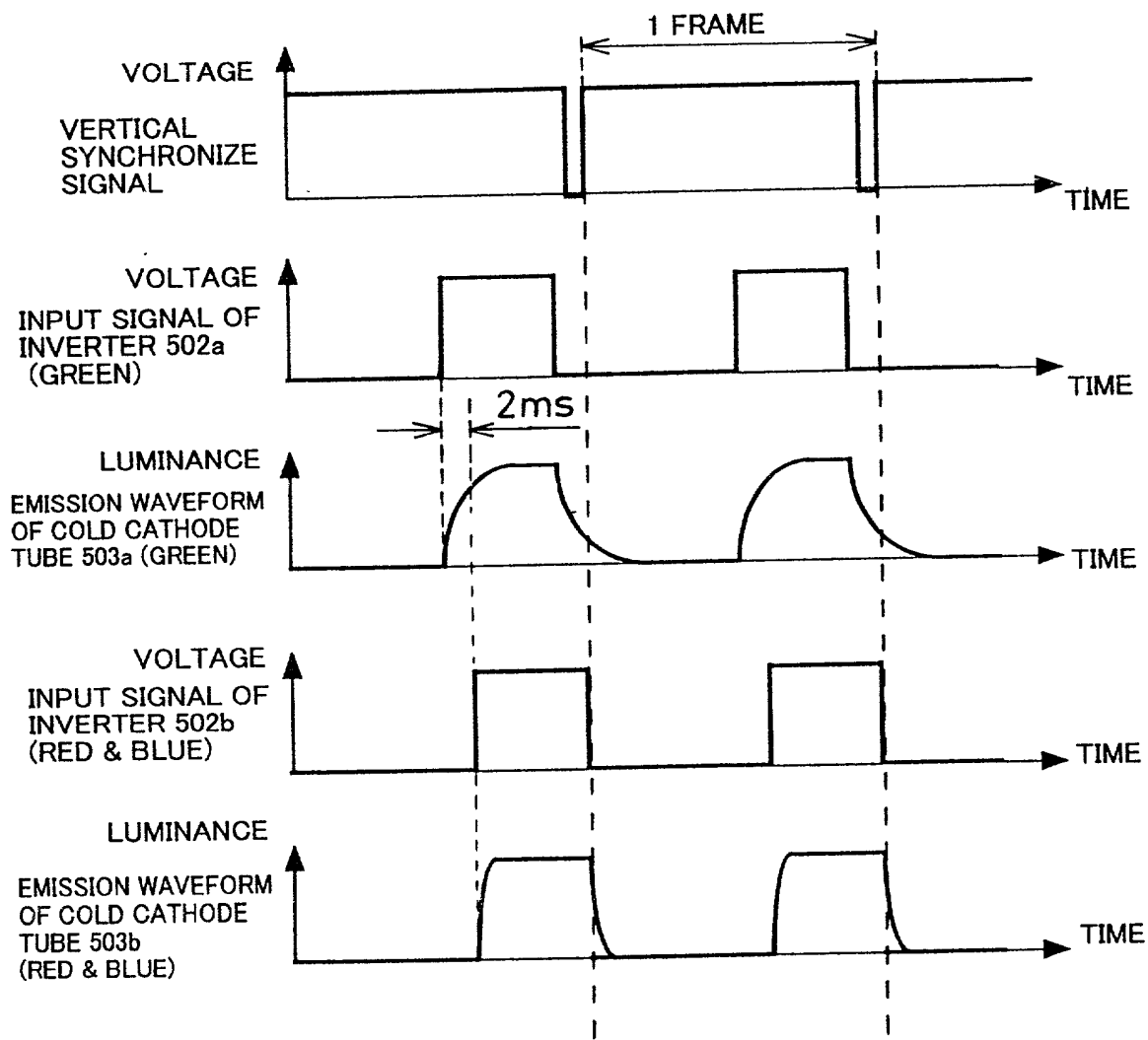


FIG. 11

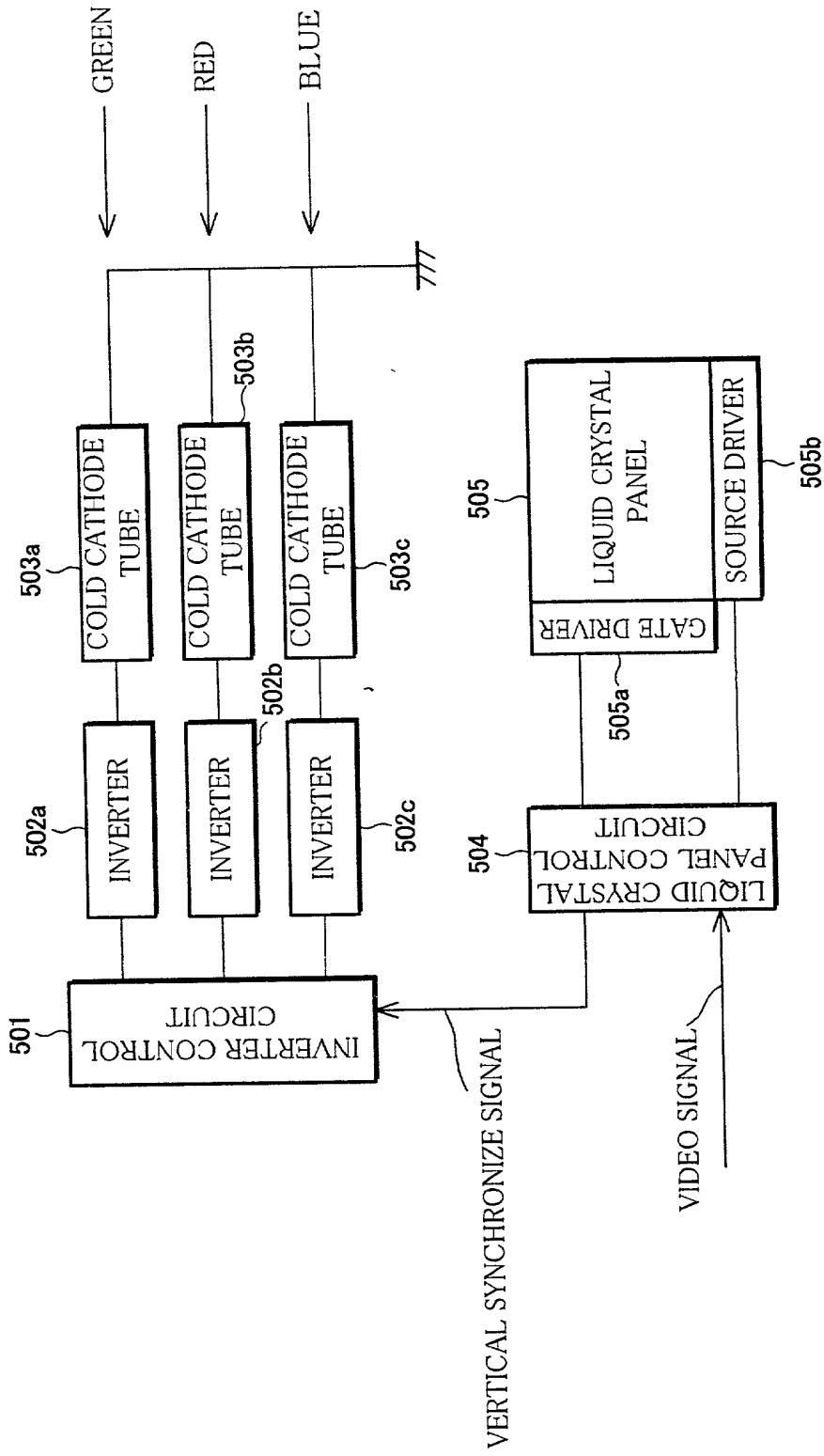


FIG. 12

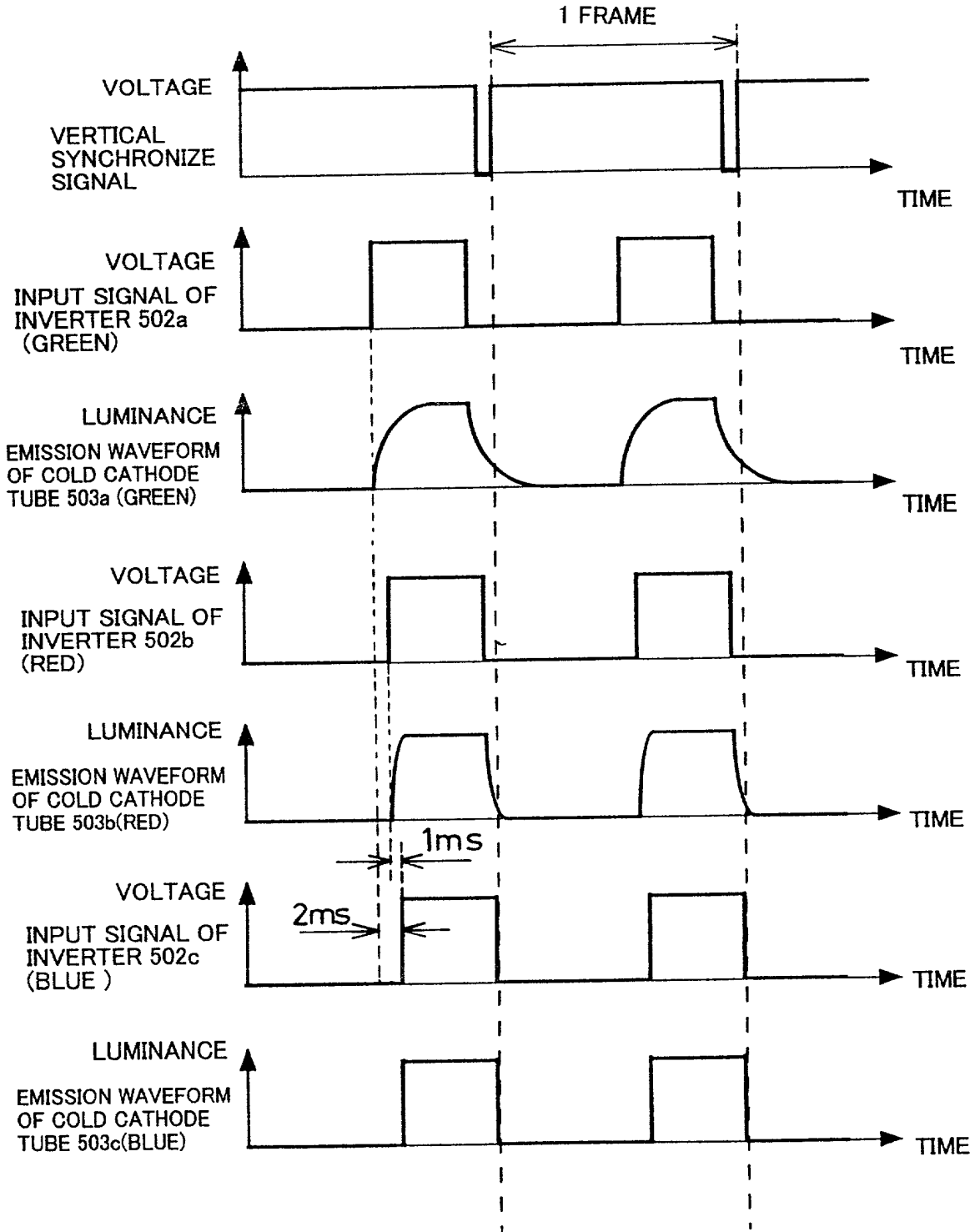


FIG. 13

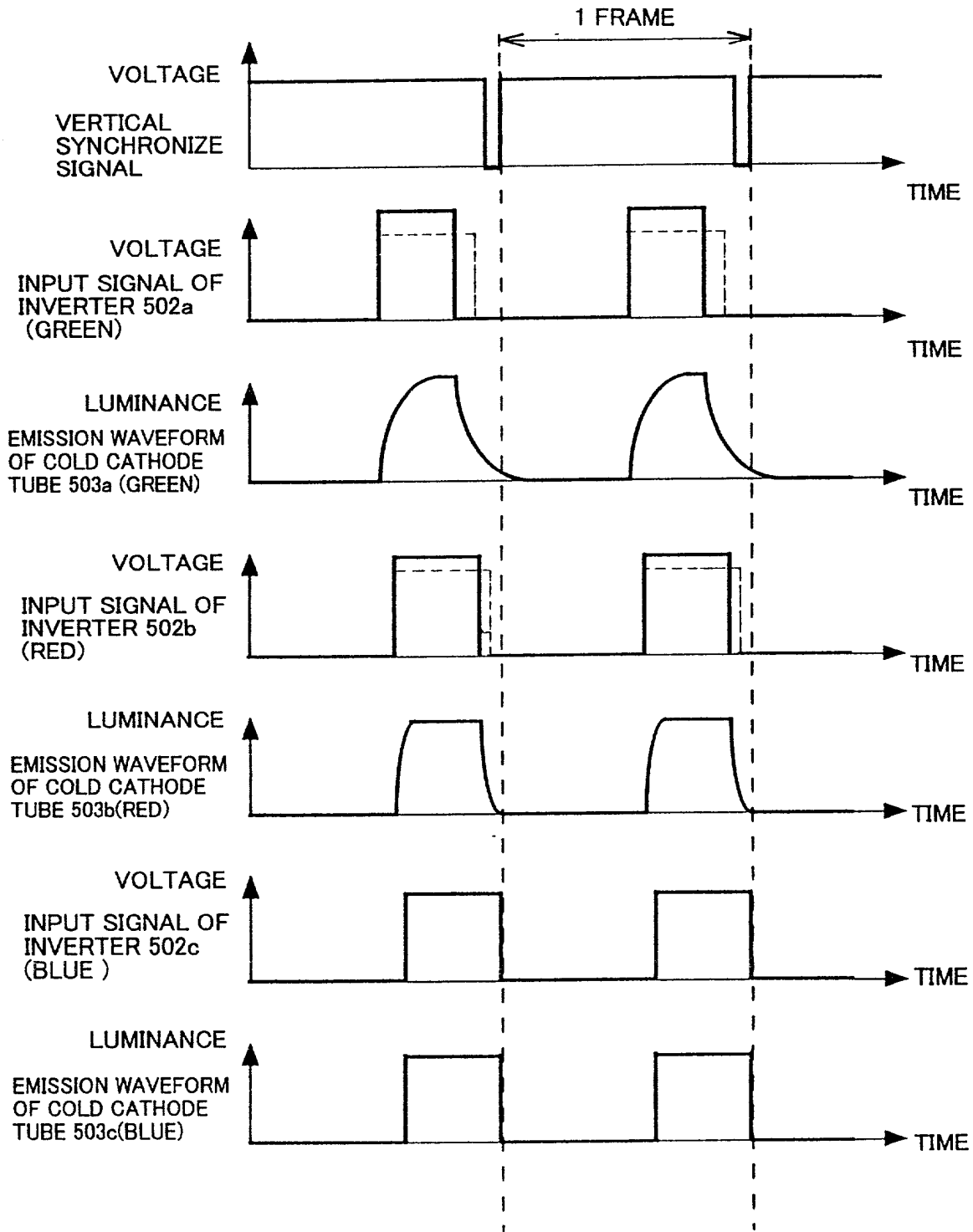


FIG. 14

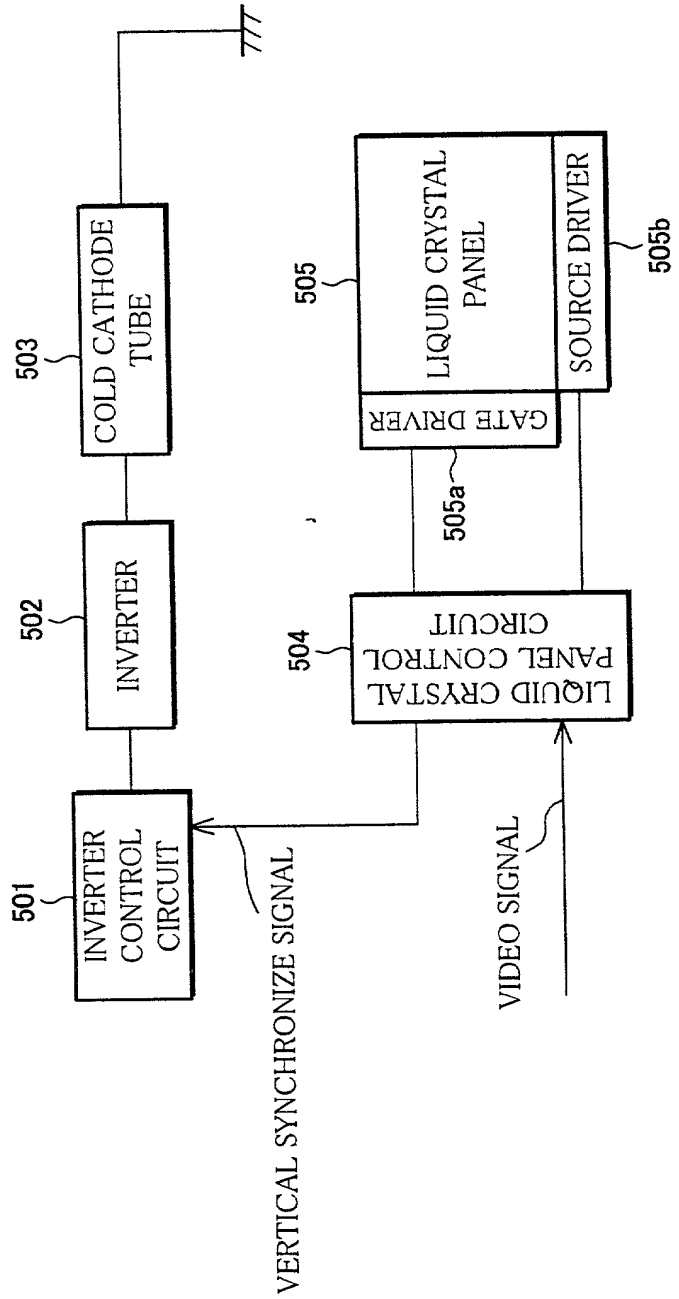
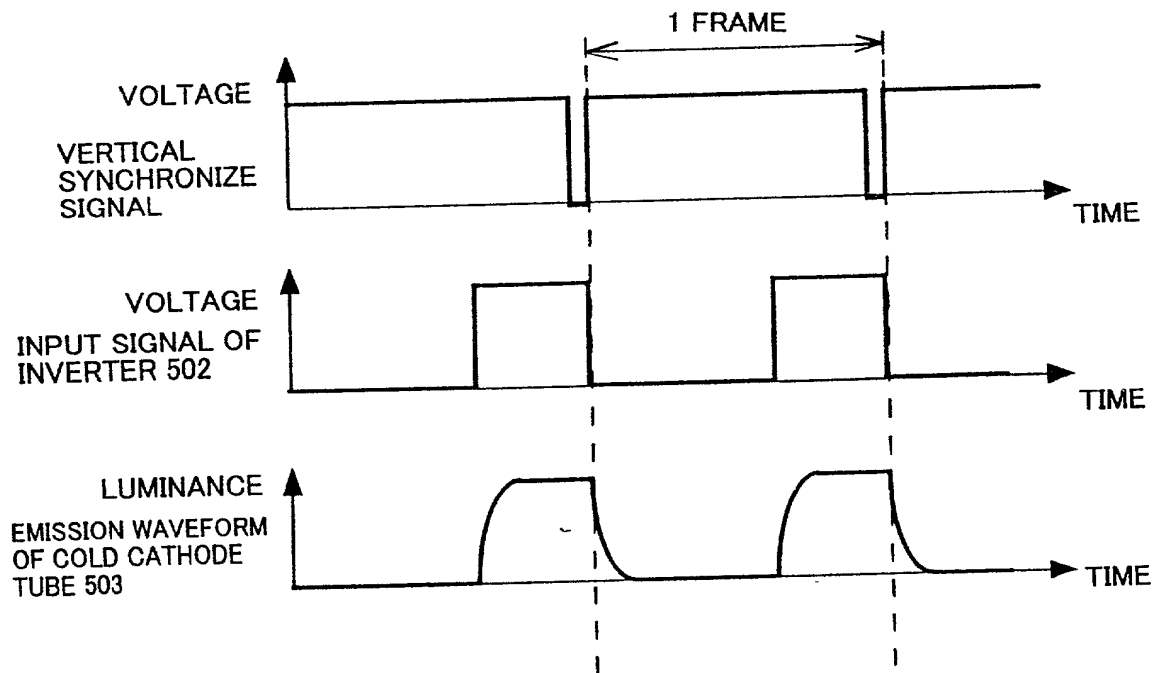
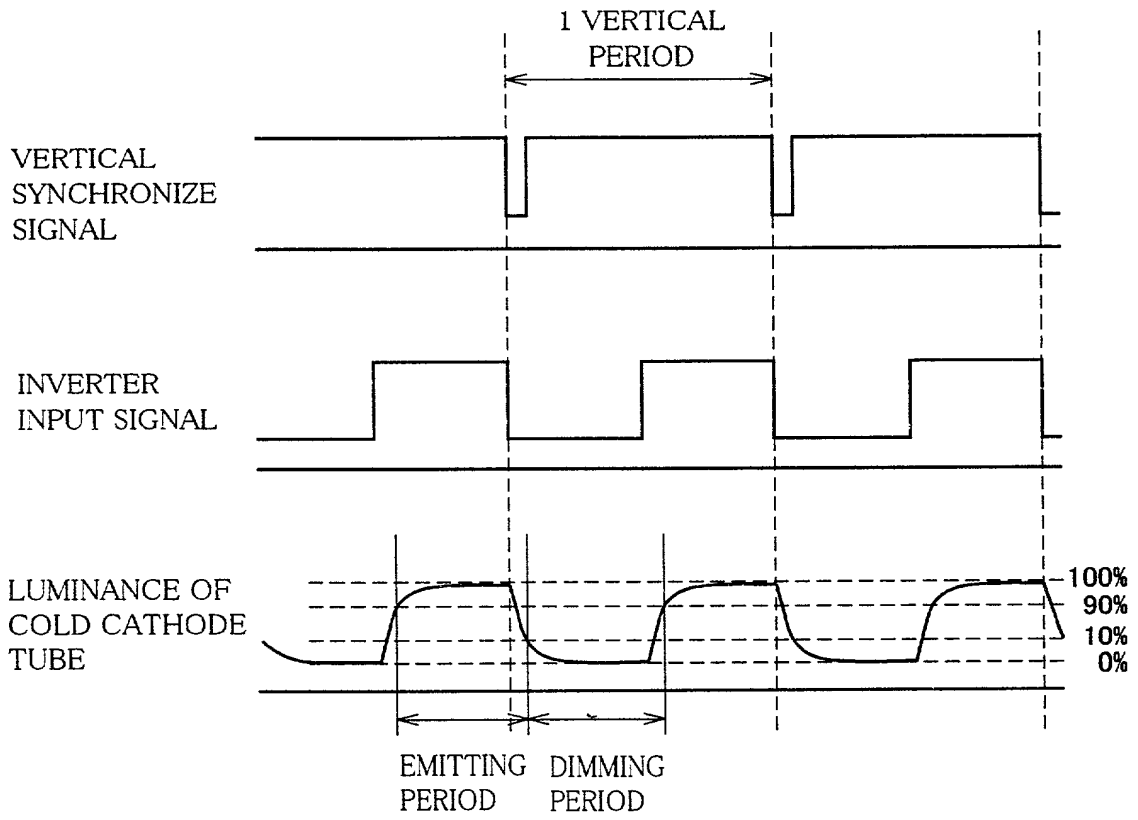


FIG. 15



Vertical Synchronize Signal

FIG. 16



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FIG. 17

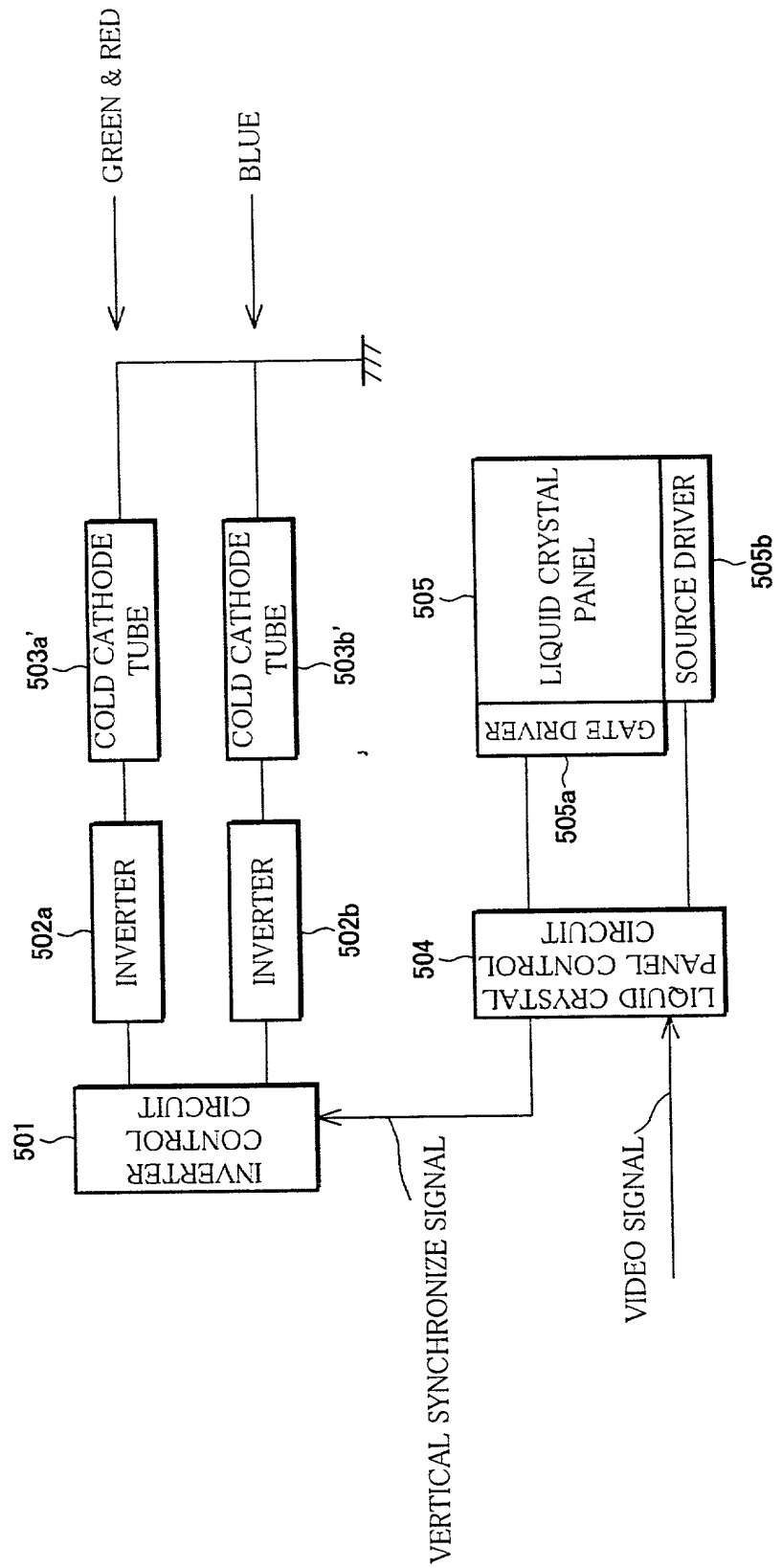
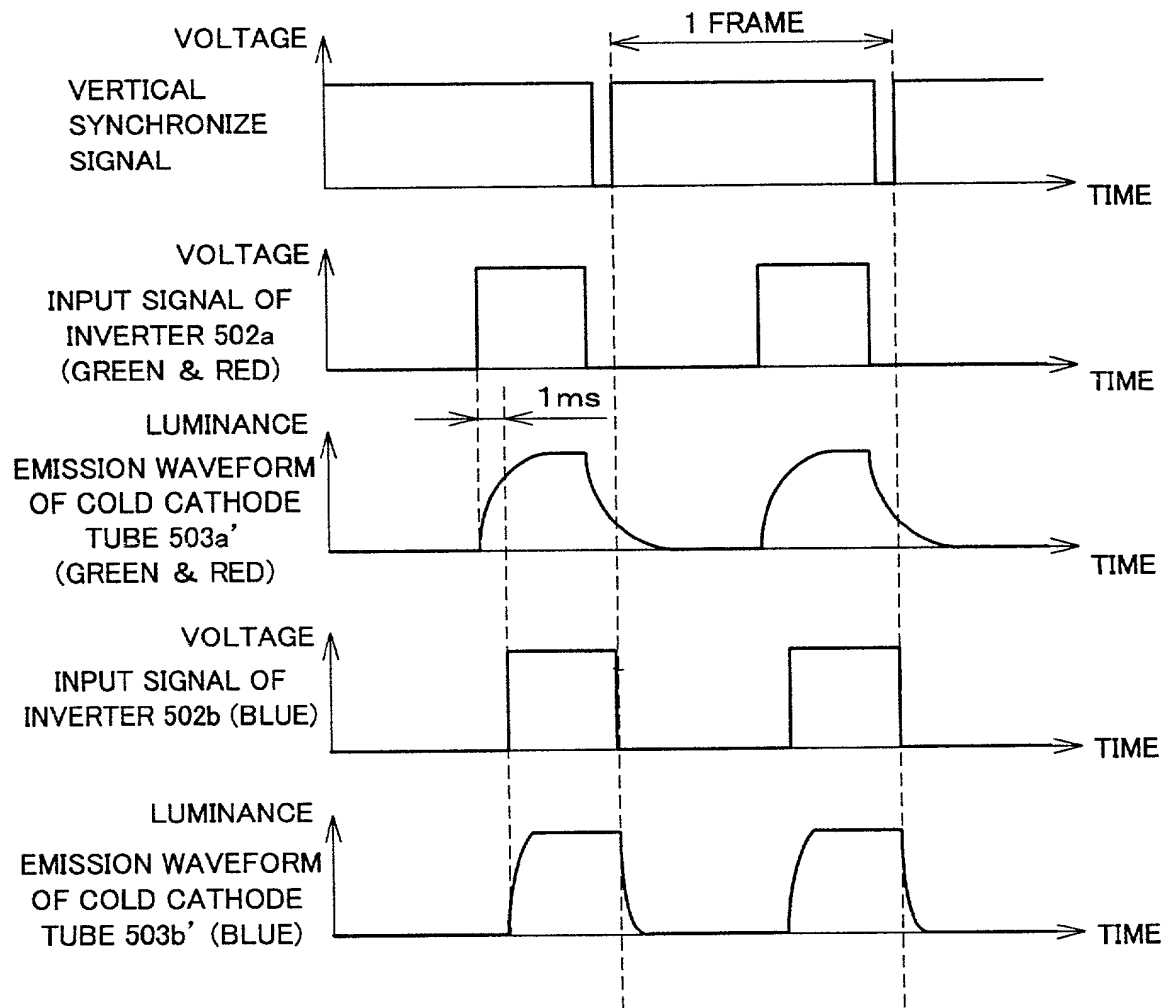


FIG. 18



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FIG. 19

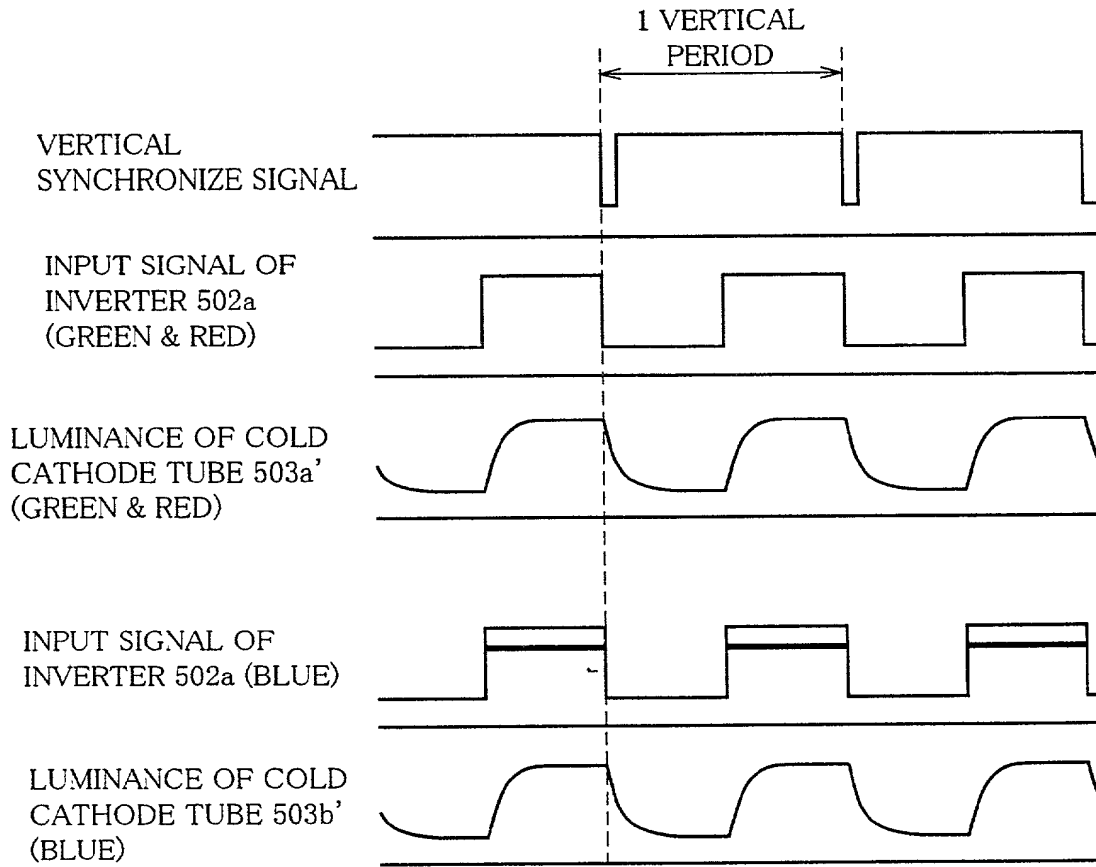


FIG. 20

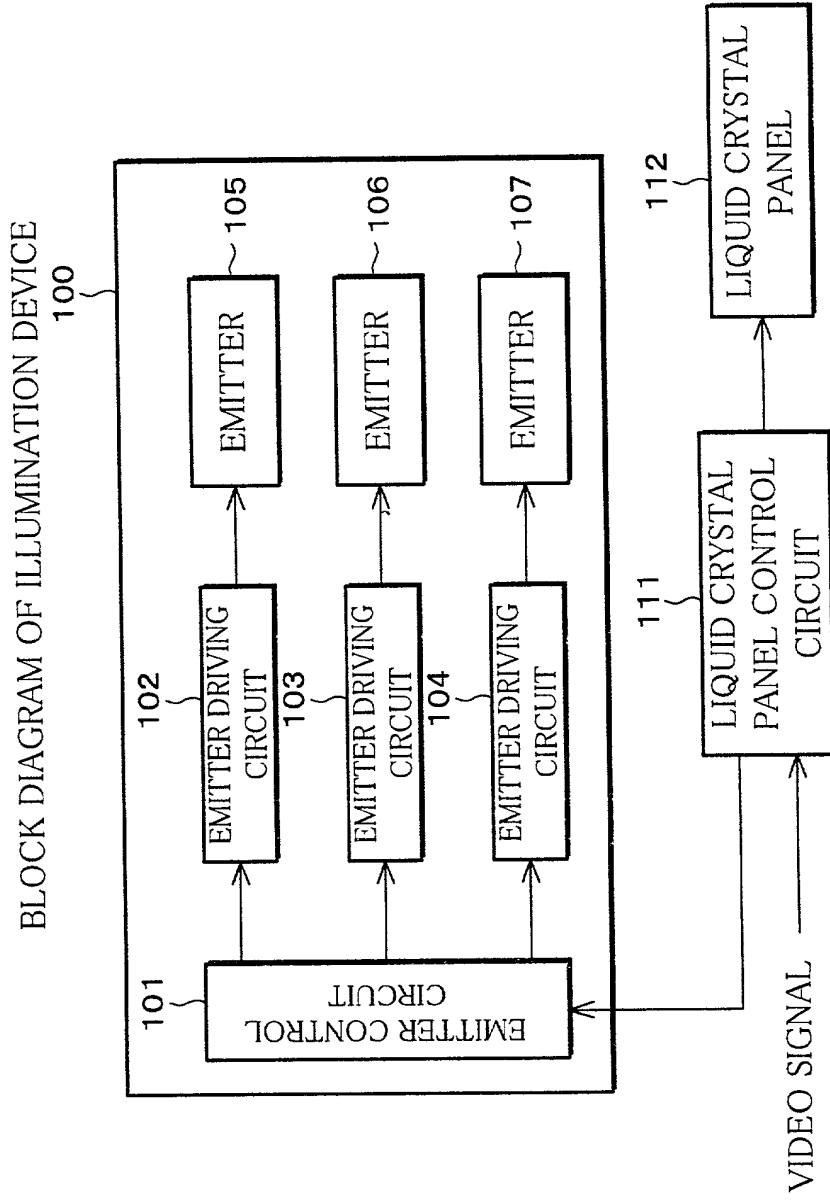
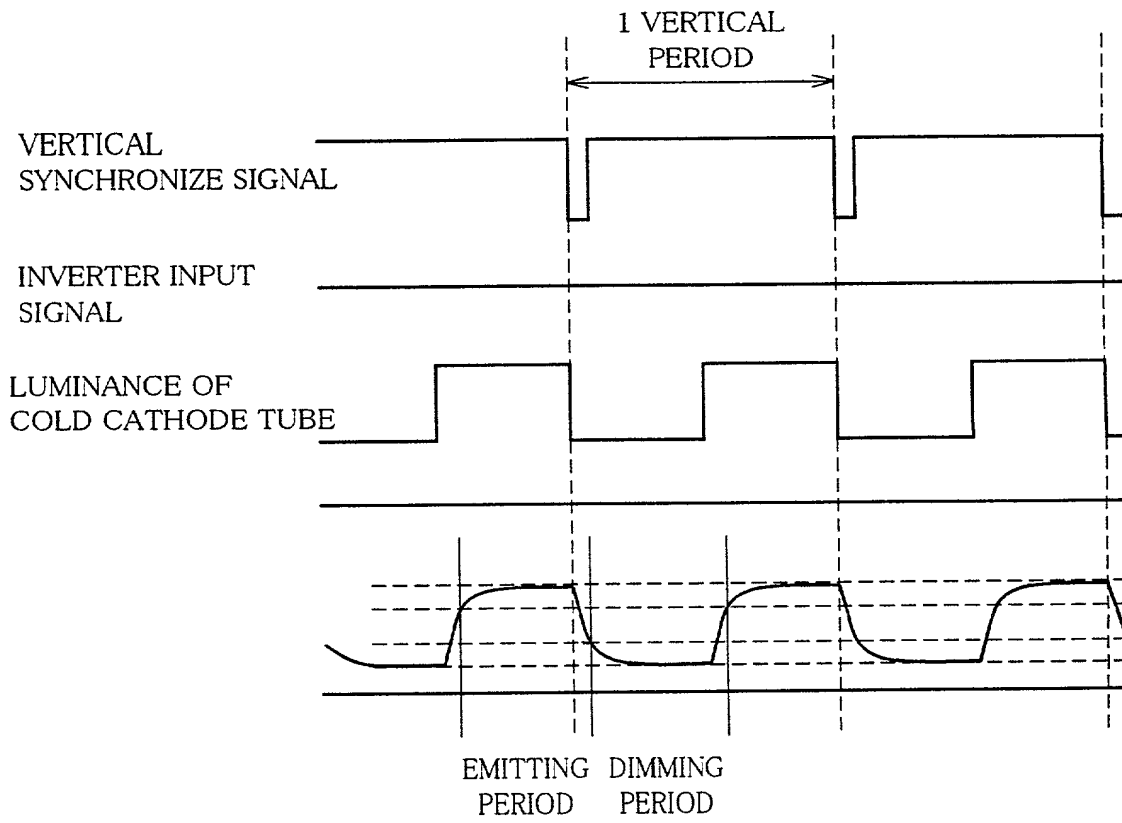
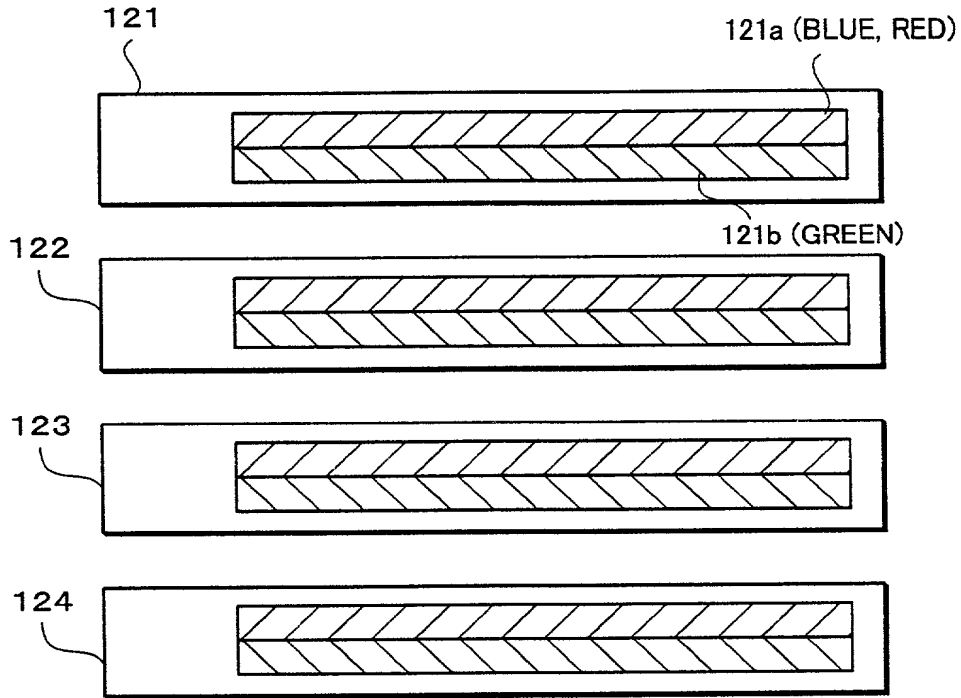


FIG. 21



F I G. 2 2 (a)



F I G. 2 2 (b)

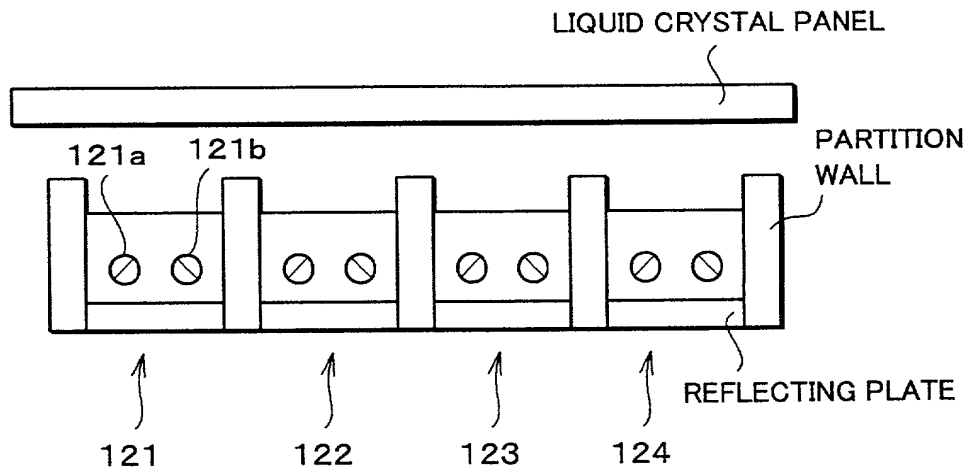


FIG. 23

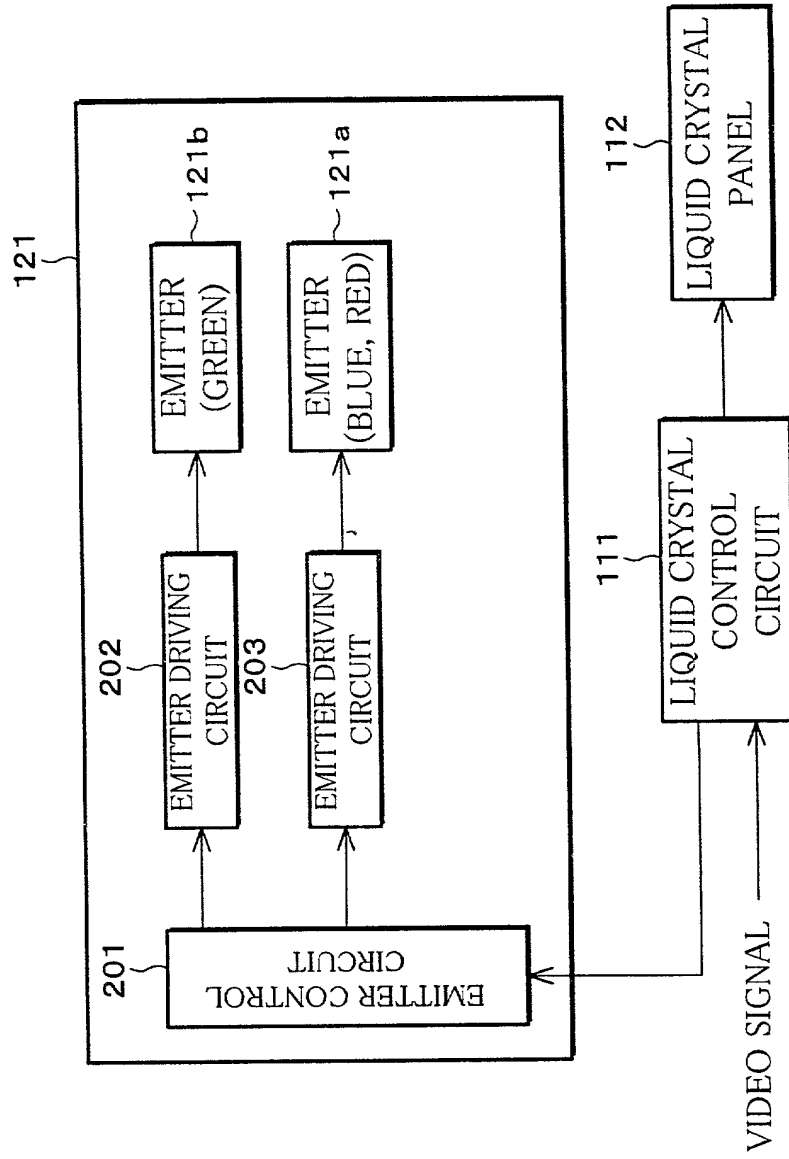


FIG. 25

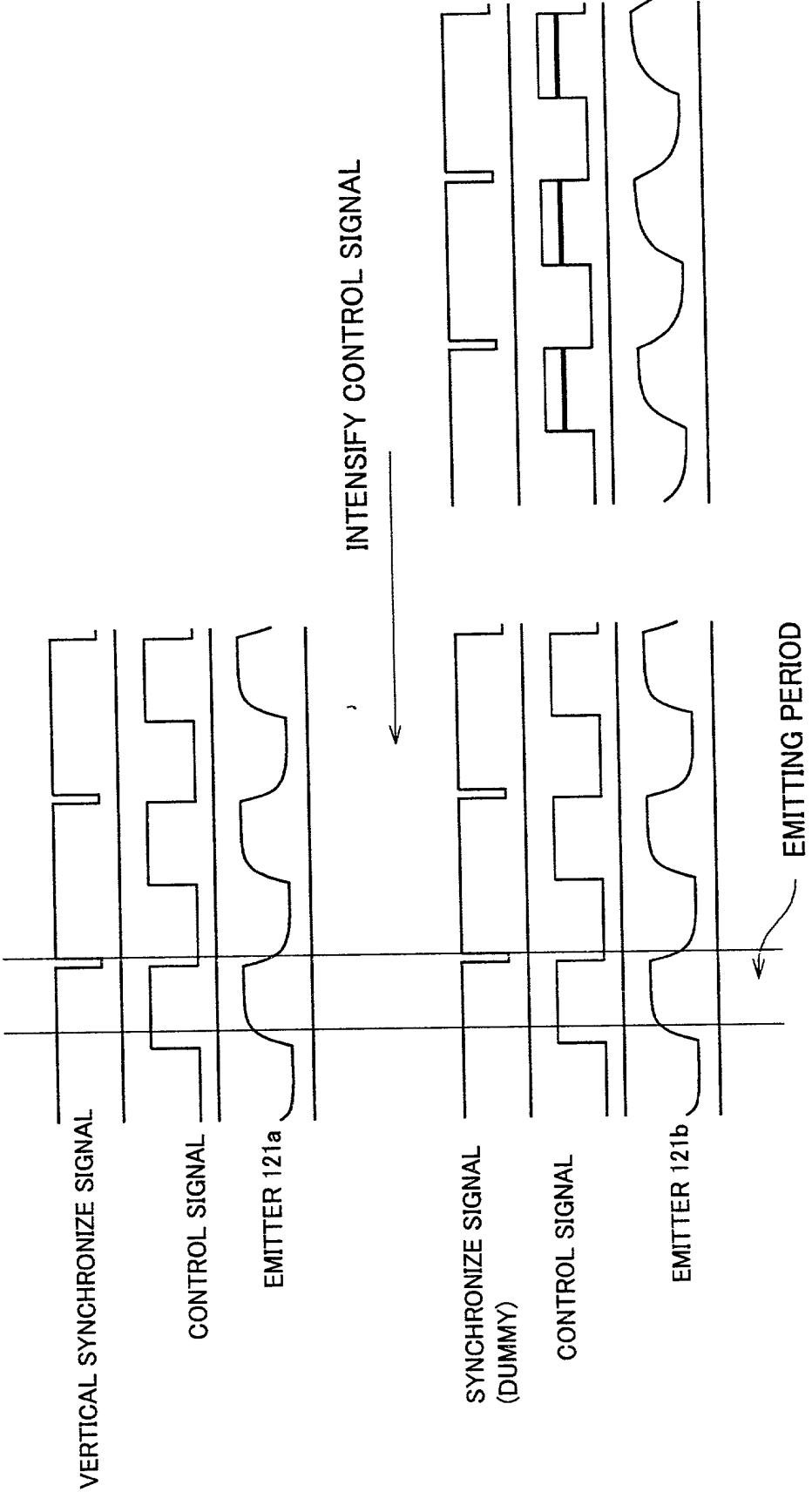


FIG. 26

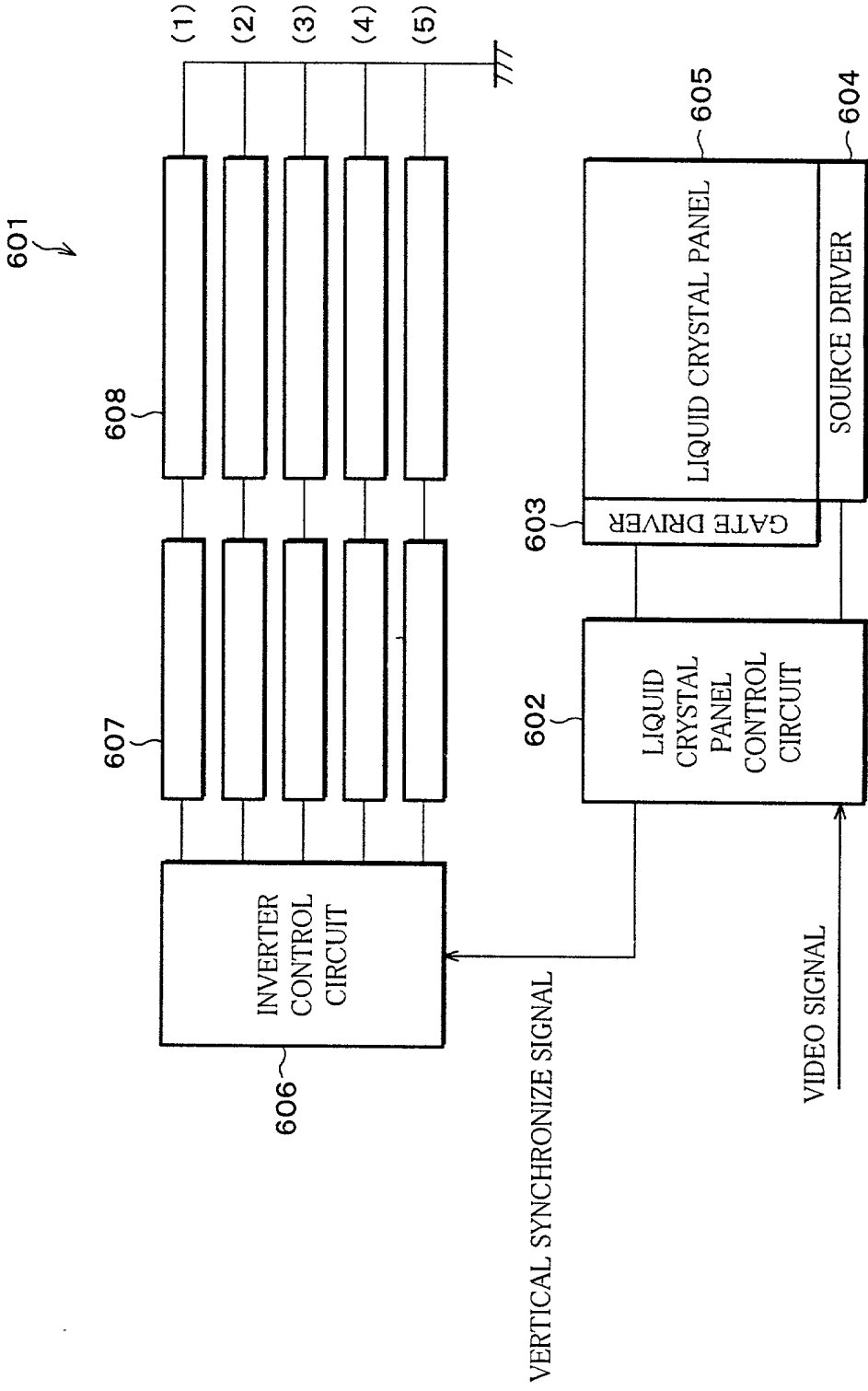


FIG. 27

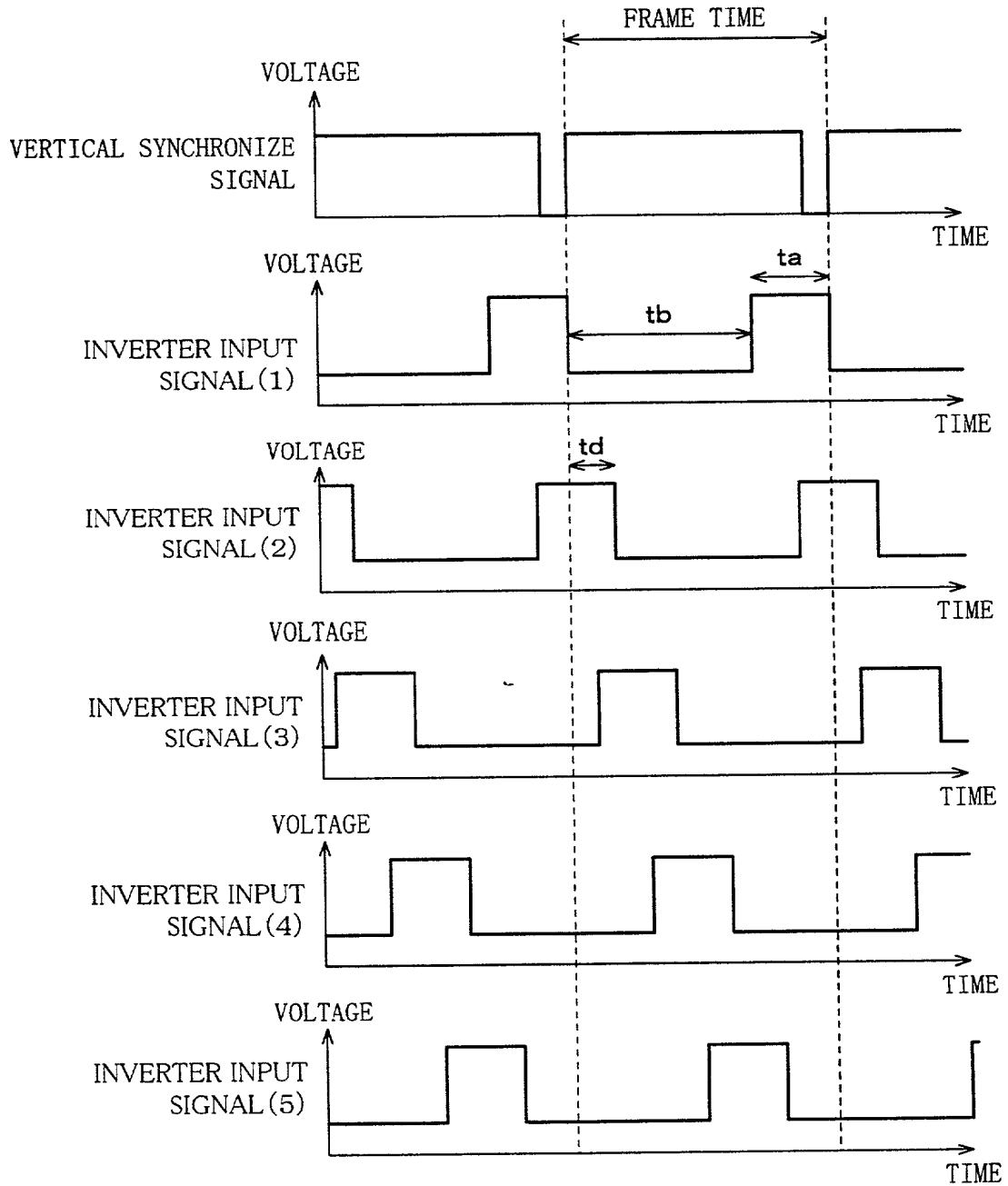


FIG. 28

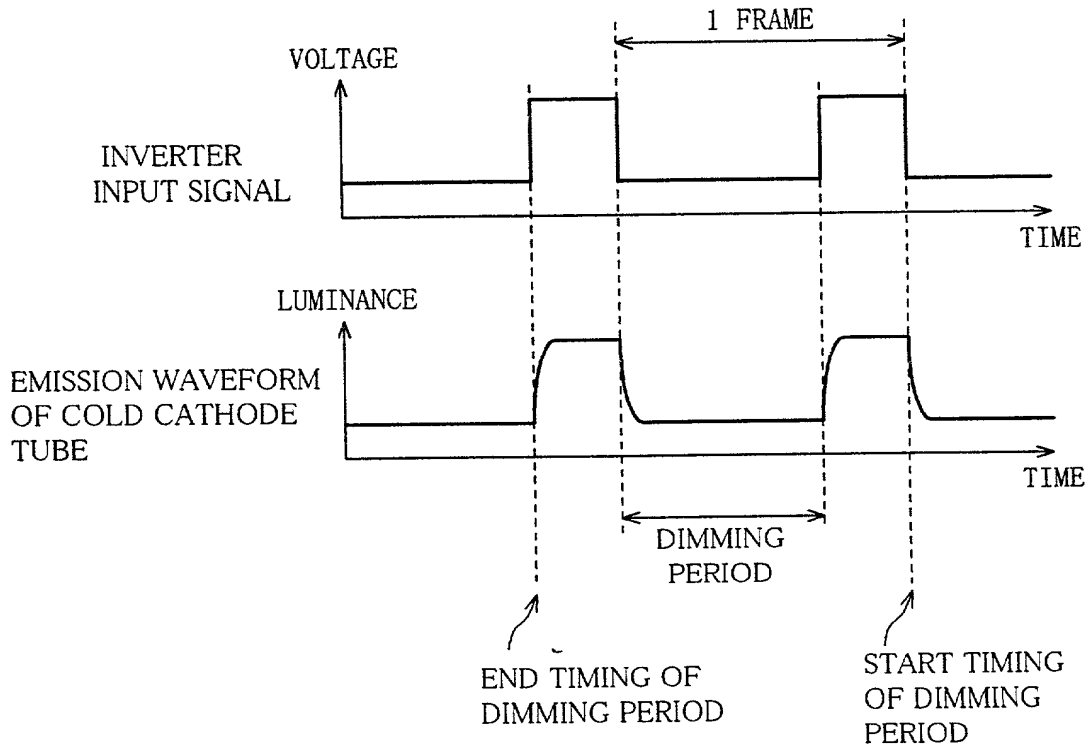


FIG. 29

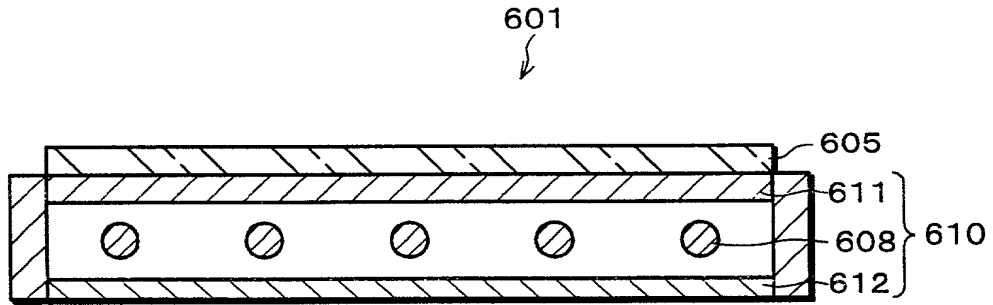


FIG. 30

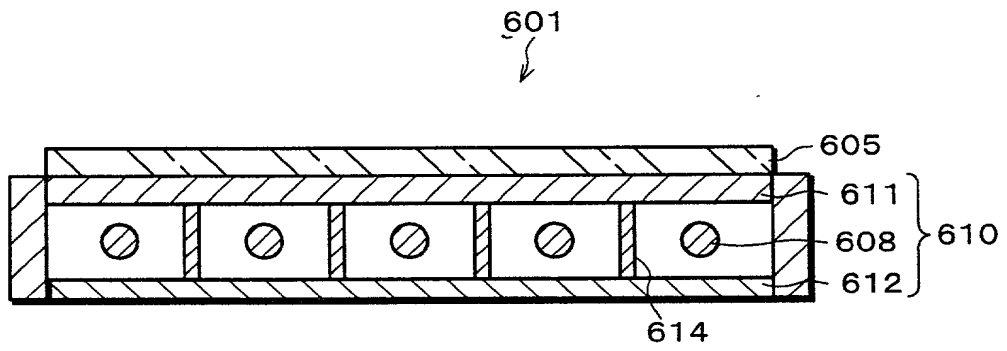


FIG. 31

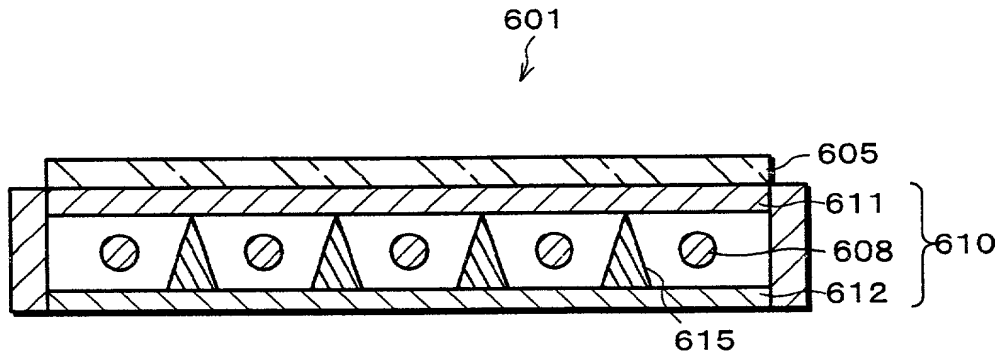


FIG. 32

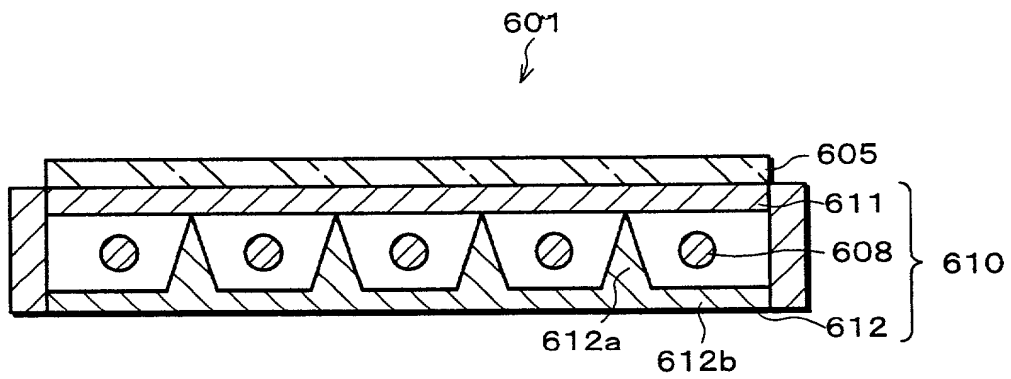


FIG. 33

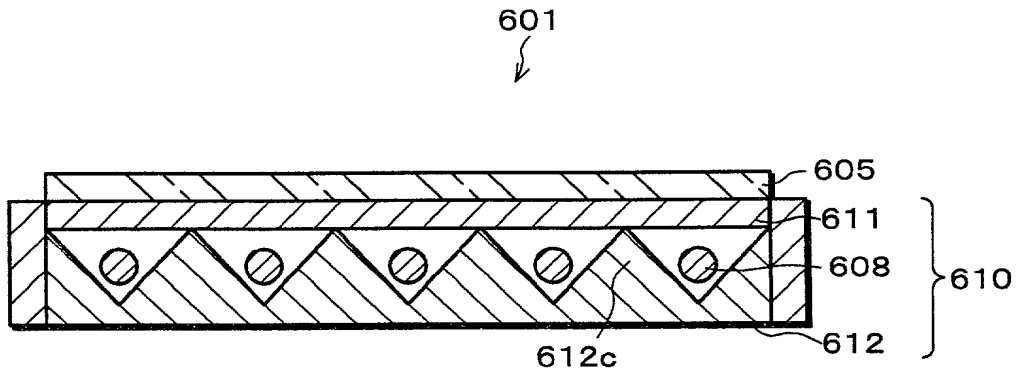
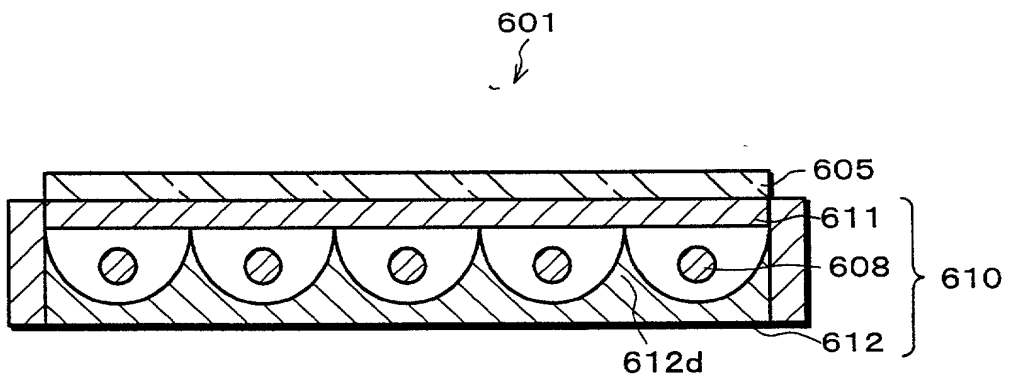


FIG. 34



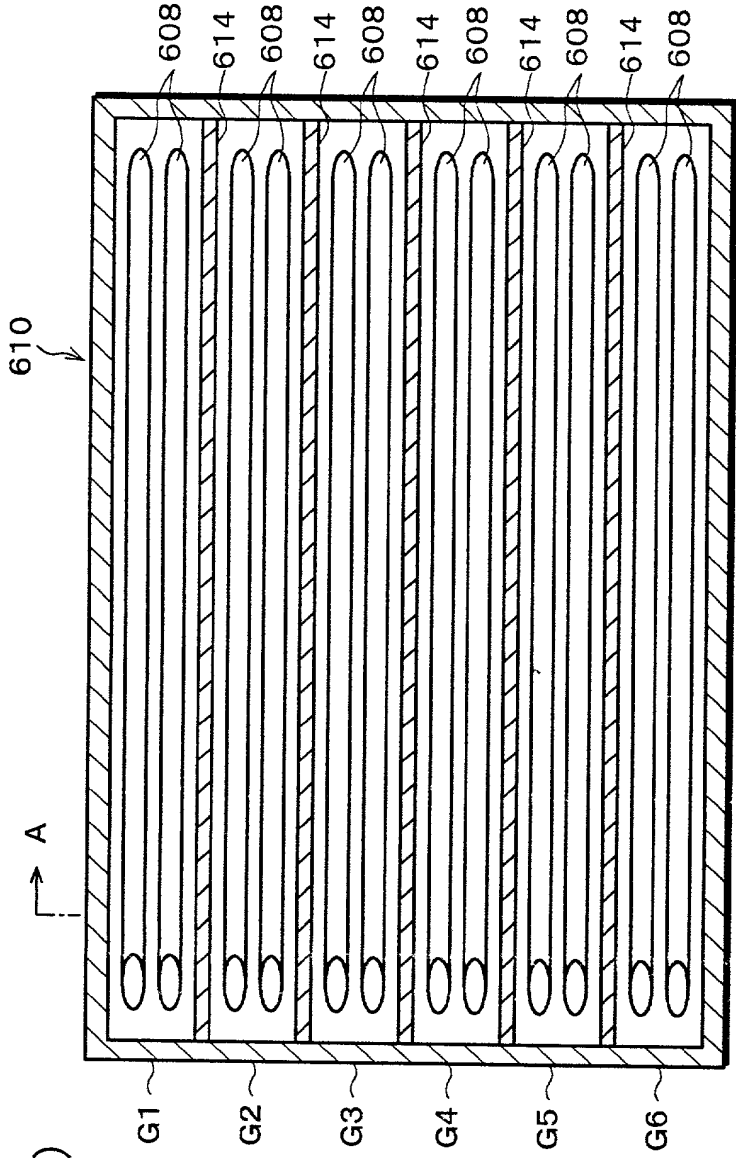


FIG. 35 (a)

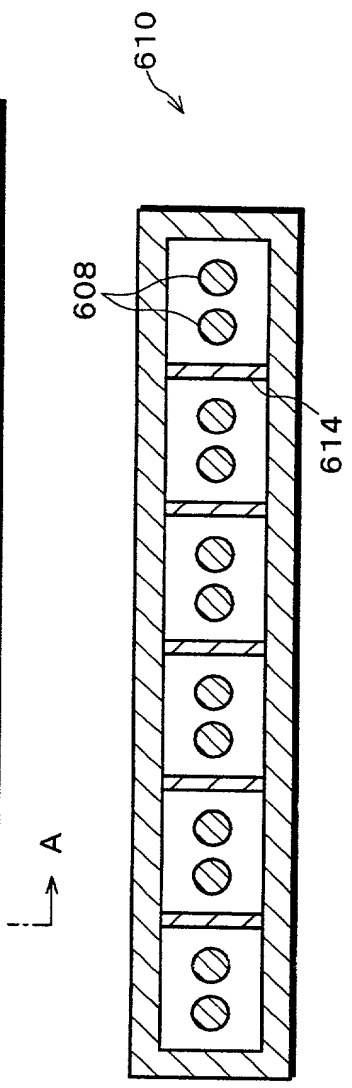


FIG. 35 (b)

FIG. 36

FIG. 36

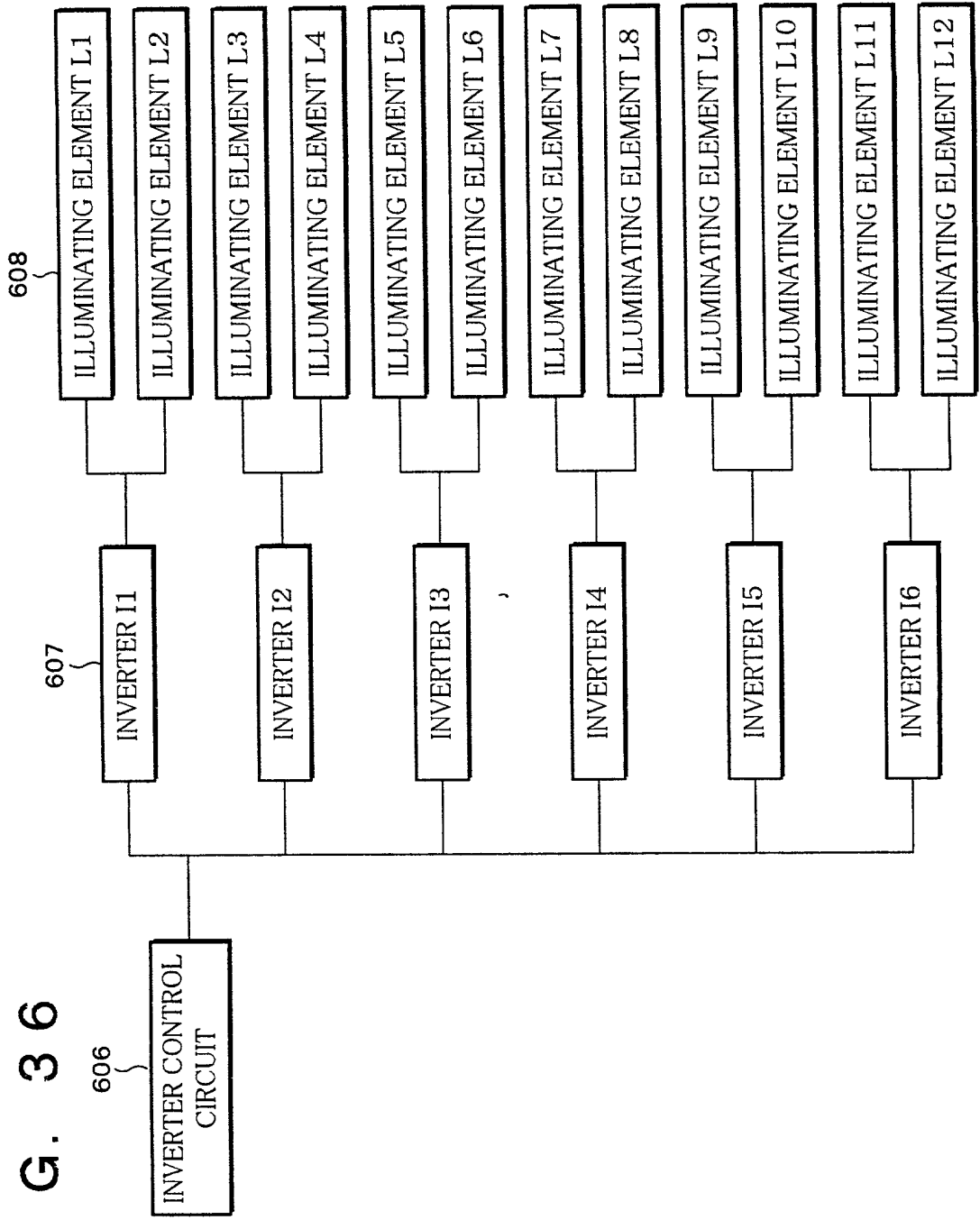


FIG. 37

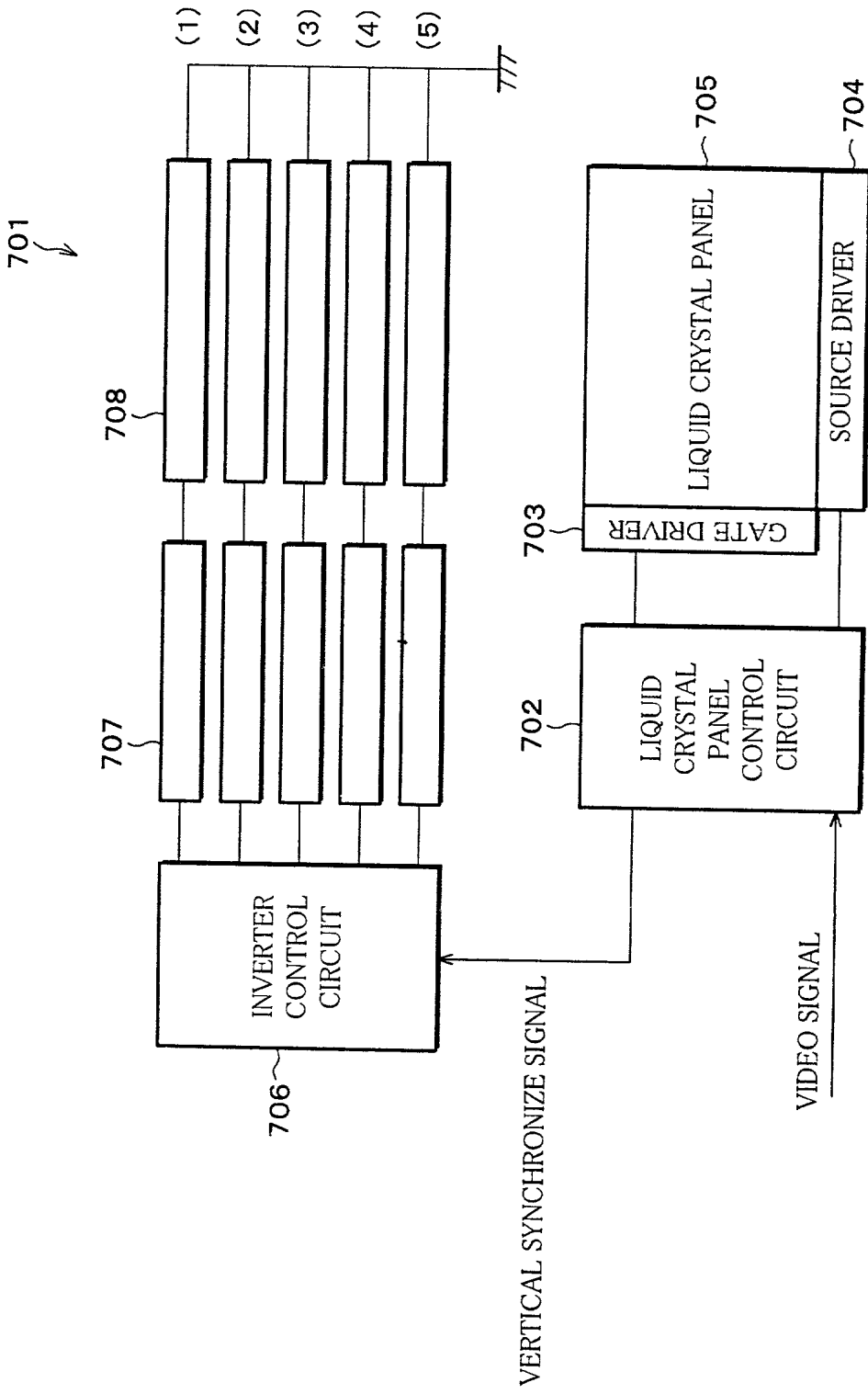


FIG. 38

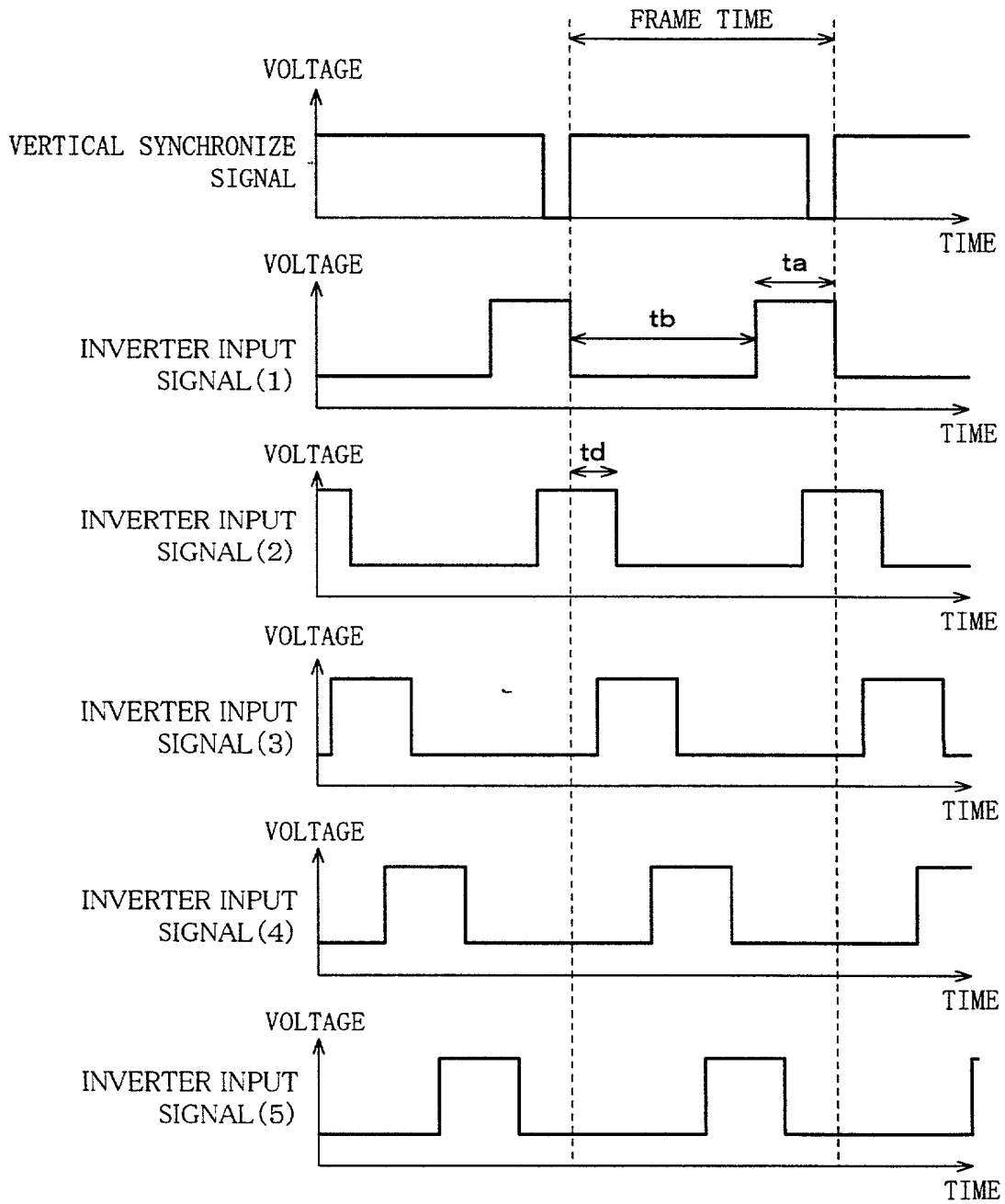


FIG. 39

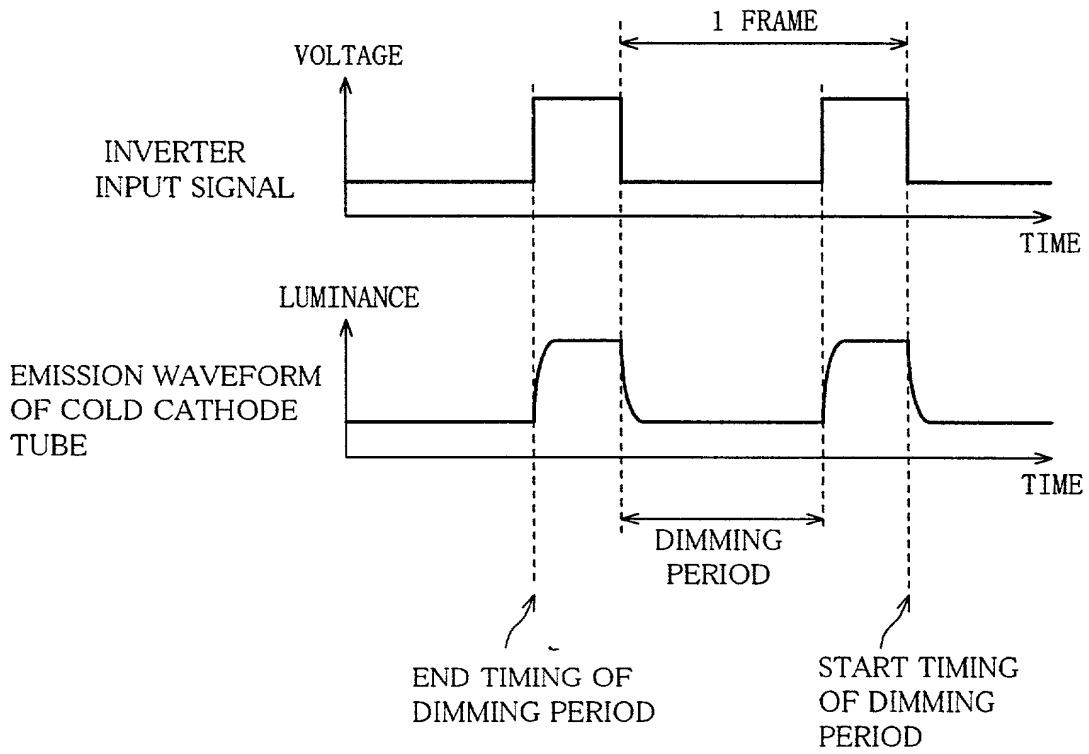


FIG. 40

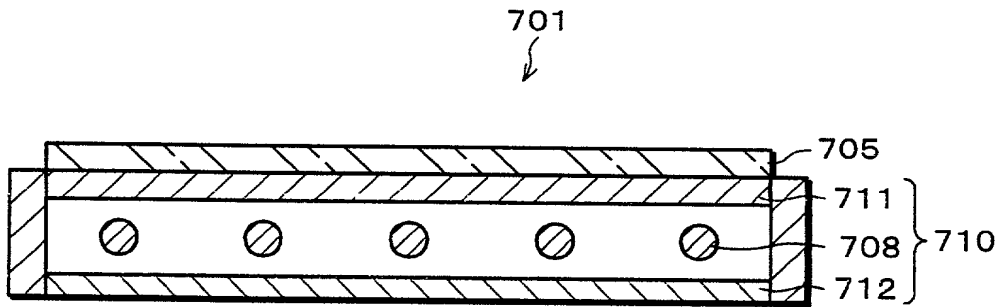


FIG. 40

FIG. 41

END TIMING OF DIMMING PERIOD	9/10	⊙	○	△	△	△	△	△	△	△	×
	8/10	⊙	○	△	△	△	△	△	△	×	○
	7/10	⊙	○	△	△	△	△	△	×	○	○
	6/10	⊙	○	△	△	△	△	×	○	○	○
	5/10	⊙	○	△	△	△	×	○	○	○	○
	4/10	○	○	△	△	×	○	○	○	○	○
	3/10	○	○	△	×	○	○	○	○	○	○
	2/10	○	○	×	○	○	○	○	○	○	○
	1/10	○	×	○	○	○	○	○	○	○	○
	0/10	×	○	△	△	△	△	△	△	△	△
	f	0/10	1/10	2/10	3/10	4/10	5/10	6/10	7/10	8/10	9/10

START TIMING OF DIMMING PERIOD

FIG. 42

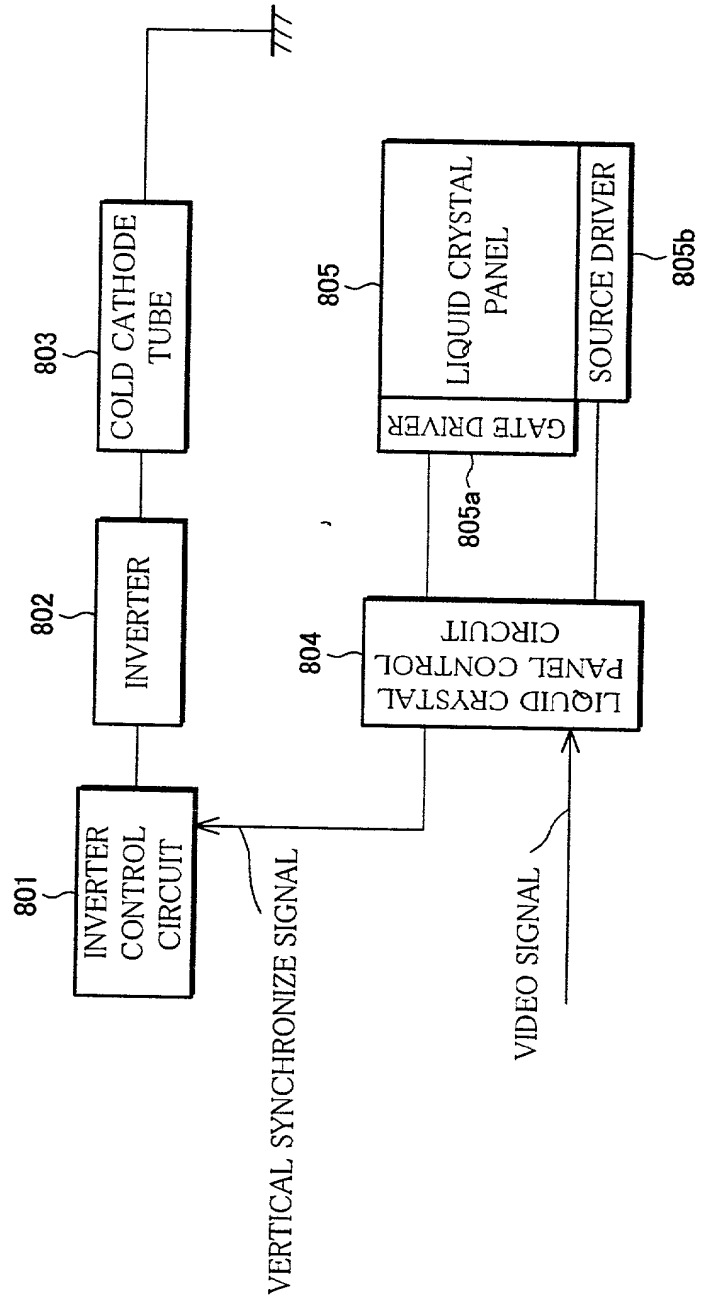


FIG. 43

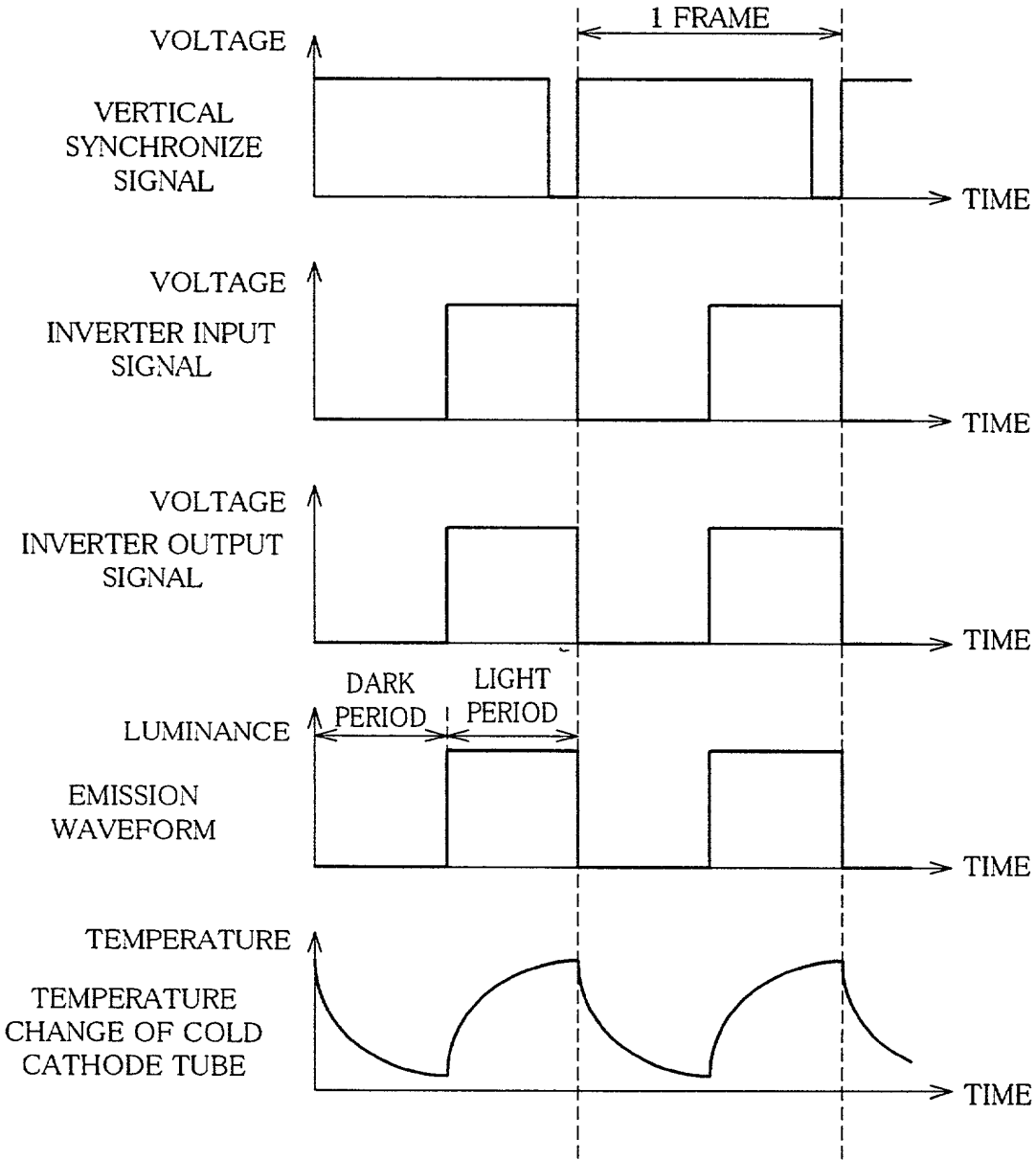
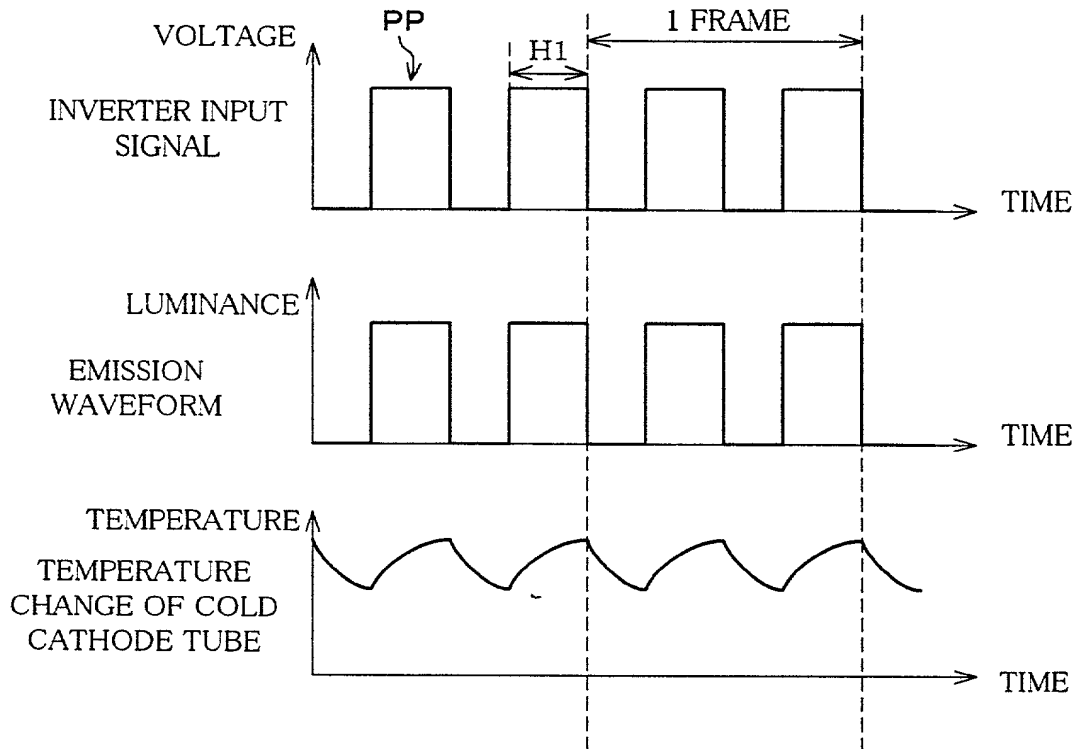


FIG. 44



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FIG. 46

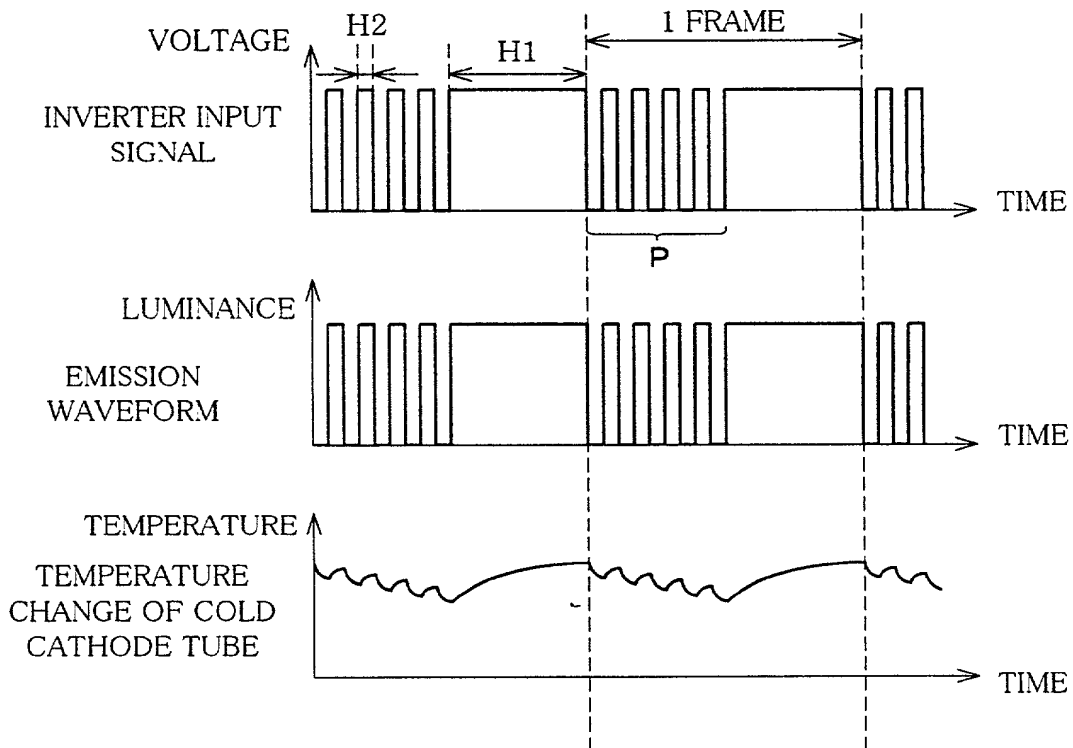


FIG. 47

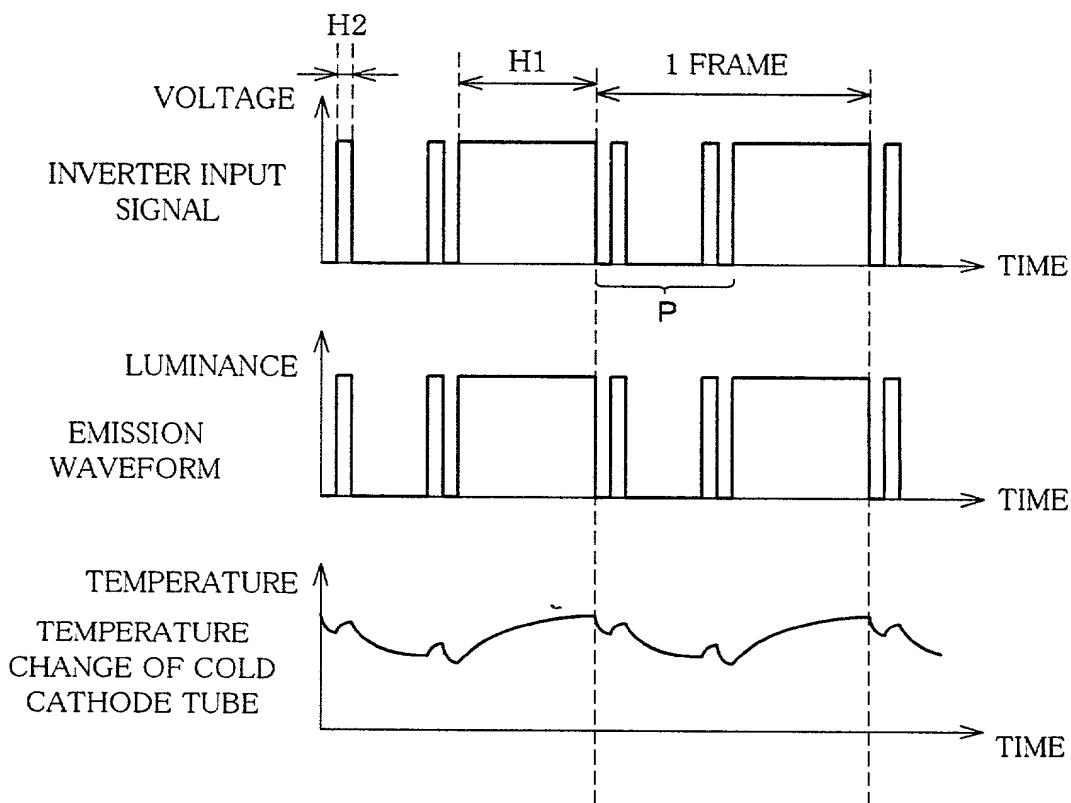


FIG. 48

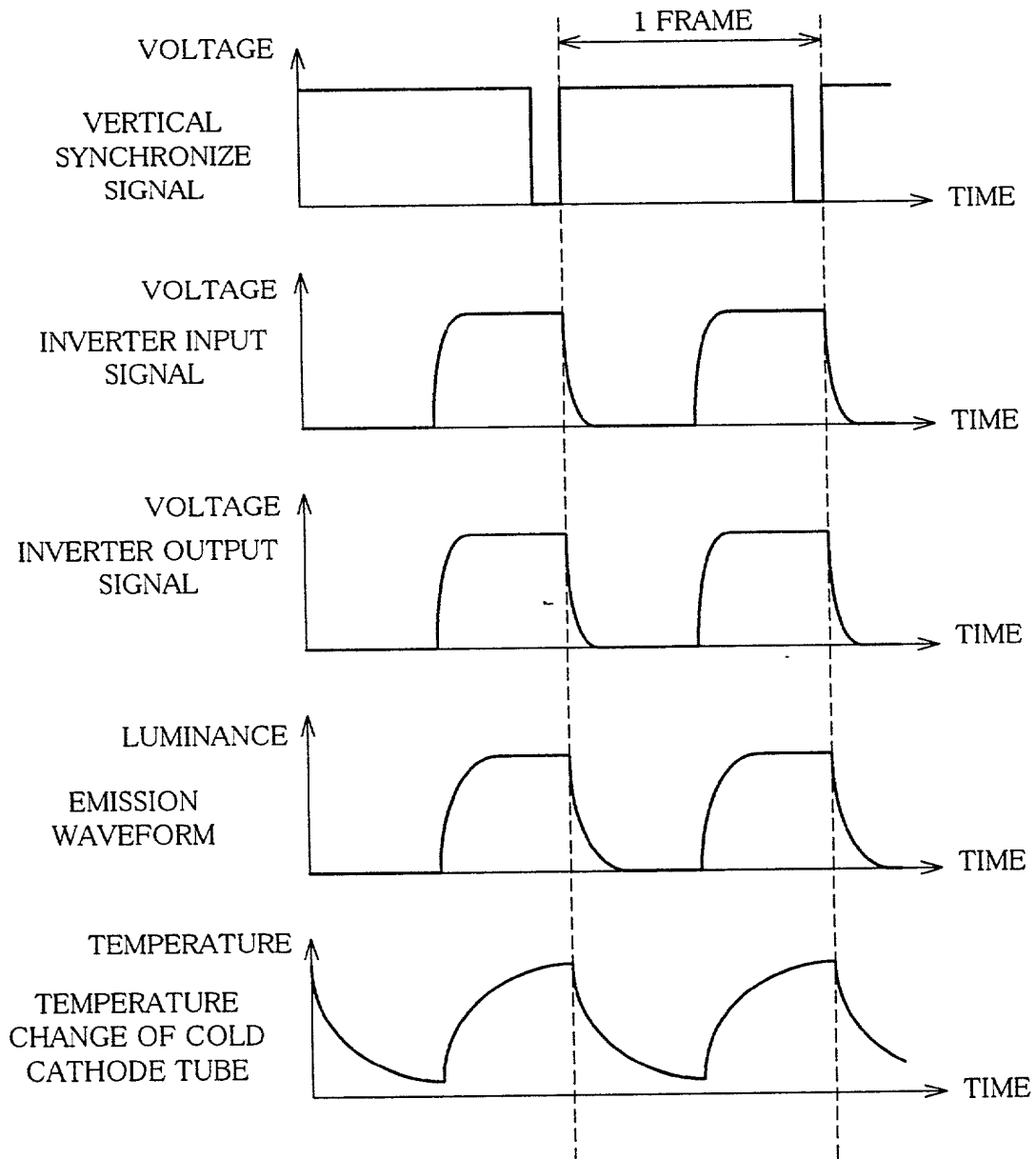


FIG. 49

